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DESIGNATED/ELECTED OFFICE (DO/EO/US)
CONCERNING A FILING UNDER 35 U.S.C. 371

XA-9593

U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR

10/031117

INTERNATIONAL APPLICATION NO.
PCT/JP00/06146INTERNATIONAL FILING DATE
8 September 2000 (08/09/00)PRIORITY DATE CLAIMED
10 September 1999 (10/09/99)

TITLE OF INVENTION

SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND PROCESS FOR PRODUCING THE SAME

APPLICANT(S) FOR DO/EO/US

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and SAEKI, Syunichi

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☐ This is an express request to begin national examination procedures (35 U.S.C. 371(f)). The submission must include items (5), (6), (9) and (24) indicated below.
4. ☒ The US has been elected by the expiration of 19 months from the priority date (Article 31).
5. ☒ A copy of the International Application as filed (35 U.S.C. 371 (c) (2))
 - a. ☐ is attached hereto (required only if not communicated by the International Bureau).
 - b. ☒ has been communicated by the International Bureau.
 - c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☒ An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)).
 - a. ☒ is attached hereto.
 - b. ☐ has been previously submitted under 35 U.S.C. 154(d)(4).
7. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371 (c)(3))
 - a. ☐ are attached hereto (required only if not communicated by the International Bureau).
 - b. ☒ have been communicated by the International Bureau.
 - c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
 - d. ☐ have not been made and will not be made.
8. ☒ An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371 (c)(4)).
10. ☐ An English language translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371 (c)(5)).
11. ☐ A copy of the International Preliminary Examination Report (PCT/IPEA/409).
12. ☒ A copy of the International Search Report (PCT/ISA/210).

Items 13 to 20 below concern document(s) or information included:

13. ☒ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
14. ☒ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
15. ☒ A **FIRST** preliminary amendment.
16. ☐ A **SECOND** or **SUBSEQUENT** preliminary amendment.
17. ☐ A substitute specification.
18. ☐ A change of power of attorney and/or address letter.
19. ☐ A computer-readable form of the sequence listing in accordance with PCT Rule 13ter.2 and 35 U.S.C. 1.821 - 1.825.
20. ☐ A second copy of the published international application under 35 U.S.C. 154(d)(4).
21. ☒ A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4).
22. ☐ Certificate of Mailing by Express Mail
23. ☒ Other items or information:

Copy of Form PCT/IB/308
23 sheets formal drawings
Letter Regarding InventorshipASSIGNEE INFORMATIONAssignee: Hitachi, Ltd.
Assignee: Hitachi Device Engineering Co., Ltd.

U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR 1.101) 10/031117		INTERNATIONAL APPLICATION NO. PCT/JP00/06146		ATTORNEY'S DOCKET NUMBER XA-9593	
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24. The following fees are submitted:

BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)) :

<input type="checkbox"/> Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO	\$1040.00
<input checked="" type="checkbox"/> International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO	\$890.00
<input type="checkbox"/> International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO	\$740.00
<input type="checkbox"/> International preliminary examination fee (37 CFR 1.482) paid to USPTO but all claims did not satisfy provisions of PCT Article 33(1)-(4)	\$710.00
<input type="checkbox"/> International preliminary examination fee (37 CFR 1.482) paid to USPTO and all claims satisfied provisions of PCT Article 33(1)-(4)	\$100.00

ENTER APPROPRIATE BASIC FEE AMOUNT =

Surcharge of **\$130.00** for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492 (e)).

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
Total claims	115 - 20 =	95	x \$18.00		\$1,710.00
Independent claims	6 - 3 =	3	x \$84.00		\$252.00
Multiple Dependent Claims (check if applicable). <input checked="" type="checkbox"/>					\$280.00
TOTAL OF ABOVE CALCULATIONS =					\$3,132.00
<input type="checkbox"/> Applicant claims small entity status. See 37 CFR 1.27. The fees indicated above are reduced by 1/2.					\$0.00
SUBTOTAL =					\$3,132.00
Processing fee of \$130.00 for furnishing the English translation later than <input type="checkbox"/> 20 <input type="checkbox"/> 30 months from the earliest claimed priority date (37 CFR 1.492 (f)).					\$0.00
TOTAL NATIONAL FEE =					\$3,132.00
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31) (check if applicable).				<input checked="" type="checkbox"/>	\$40.00
TOTAL FEES ENCLOSED =					\$3,172.00
					Amount to be: refunded \$
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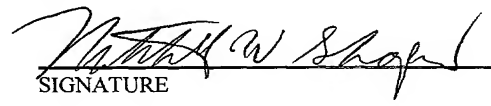
c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 50-1165. A duplicate copy of this sheet is enclosed.

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NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

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Mitchell W. Shapiro
 NAME

31,568
 REGISTRATION NUMBER

January 16, 2002
 DATE

XA-9593

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

Takashi KOBAYASHI et al

Intl. Appln. No.: PCT/JP00/06146

Intl. Filing Date: 8 September 2000

For: SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND PROCESS
FOR PRODUCING THE SAME

* * *

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Prior to examination, please amend the above-identified
patent application as indicated below.

IN THE CLAIMS:

9. (Amended) A process according to any one of Claims
1-5, 7, or 8, wherein the third gates are self-aligned to the
floating gates.

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10. (Amended) A process according to any one of Claims 1-5, 7, or 8, wherein the floating gates are self-aligned to the third gates.

24. (Amended) A process for producing a semiconductor integrated circuit device according to any one of claims 19-21 or 23, wherein the polycrystalline silicon film has a film thickness thinner than that of the first pattern which becomes the floating gates.

32. (Amended) A process for producing a semiconductor integrated circuit device according to any one of claims 14-21, 23, or 25-31, wherein the third gates are formed as self-aligned to the floating gates.

33. (Amended) A process for producing a semiconductor integrated circuit device according to any one of claims 14-21, 23, or 25-31, wherein the floating gates are formed as self-aligned to the third gates.

Please add the following claims:

40. (New) A process according to claim 6, wherein the third gates are self-aligned to the floating gates.

41. (New) A process according to claim 6, wherein the floating gates are self-aligned to the third gates.

42. (New) A process for producing a semiconductor integrated circuit device according to claim 22, wherein the polycrystalline silicon film has a film thickness thinner than that of the first pattern which becomes the floating gates.

43. (New) A process for producing a semiconductor integrated circuit device according to claim 22, wherein the third gates are formed as self-aligned to the floating gates.

44. (New) A process for producing a semiconductor integrated circuit device according to claim 22, wherein the floating gates are formed as self-aligned to the third gates.

45. (New) A process for producing a semiconductor integrated circuit device according to claim 24, wherein the third gates are formed as self-aligned to the floating gates.

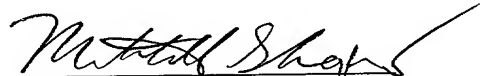
46. (New) A process for producing a semiconductor integrated circuit device according to claim 24, wherein the floating gates are formed as self-aligned to the third gates.

REMARKS

Claims 9, 10, 24, 32, and 33 have been amended to eliminate the improper multiple dependencies. Claims 40-46 correspond to the dependencies eliminated from the amended claims.

The Commissioner is hereby authorized to charge to Deposit Account No. 50-1165 any fees that may be required by this paper and to credit any overpayment to that Account. If any extension of time is required in connection with the filing of this paper and has not been requested separately, such extension is hereby requested.

Respectfully submitted,

By: 
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January 16, 2002

Marked-Up Copy of Claims -- PCT/JP00/06146

9. (Amended) A process according to any one of Claims [1 to 8] 1-5, 7, or 8, wherein the third gates are self-aligned to the floating gates.

10. (Amended) A process according to any one of Claims [1 to 8] 1-5, 7, or 8, wherein the floating gates are self-aligned to the third gates.

24. (Amended) A process for producing a semiconductor integrated circuit device according to any one of claims [19 to 23] 19-21 or 23, wherein the polycrystalline silicon film has a film thickness thinner than that of the first pattern which becomes the floating gates.

32. (Amended) A process for producing a semiconductor integrated circuit device according to any one of claims [14 to 31] 14-21, 23, or 25-31, wherein the third gates are formed as self-aligned to the floating gates.

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33. (Amended) A process for producing a semiconductor integrated circuit device according to any one of claims [14 to 31] 14-21, 23, or 25-31, wherein the floating gates are formed as self-aligned to the third gates.

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DESCRIPTION

SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE
AND PROCESS FOR PRODUCING THE SAME

Technical Field

The present invention relates to a semiconductor integrated circuit device and a process for producing the same, and particularly to a technique of realizing integration, reliability improvement and low voltage operation at a high speed of a nonvolatile semiconductor memory device capable of electrically programming/erasing.

Background Art

Among nonvolatile semiconductor memory devices capable of electrically programming/erasing, the so-called flash memory capable of bulk erasing is well known. Flash memory is distinguished in mobility and impact resistance and is capable of electrically conducting bulk erasing and thus is now in rapidly increasing demand as the file (memory device) of personal digital assistants such as mobile personal computers, digital still cameras, etc. Reduction in bit cost by reducing the memory cell area is an important factor in the market expansion. For example, as disclosed in Ohyobutsuri, 65, No. 11, 1114-1124, published by Japan Society of Applied Physics (Ohyobutsuri-Gakkai) on November 10, 1996, various

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memory cell systems have been proposed for its realization.

On the other hand, Japanese Patent No. 2,694,618 (Reference 1) discloses a virtual ground type memory cell using three-layered polysilicon gates. That is, the memory cells each comprise a semiconductor region and three kinds of gates formed on a well in a semiconductor substrate. Three kind of gates are a floating gate formed on the well, a control gate formed on the floating gate and an erase gate formed between the adjacent control gate and floating gate. The three kinds of gates are made of polysilicon and isolated from one another by insulator films, respectively, and the floating gate and the well are also isolated from each other by another insulator film. The control gates are connected in the row direction (direction x) to form word lines. Source/drain diffusion layers are formed in the column direction as a virtual ground type, sharing with the adjacent memory cell and diffusion layer to attain pitch reduction in the column direction. The erase gates are arranged in parallel to channels and also in parallel to the word lines and between the word lines (control gates).

In the programming of the memory cells as described in Reference 1, a positive voltage is mutually independently applied to the word lines and the drains, whereas the well, the sources and the erase gates are maintained at zero (0) volt, whereby hot

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electrons are generated in the channel regions near the drains, and electrons are injected into the floating gates to elevate the threshold voltage of the memory cells. In the erasing, a positive voltage is applied to the erase gates, whereas the word lines, the sources and the well are maintained at zero (0) V, whereby electrons are emitted from the floating gates to the erase gates to lower the threshold voltage.

Furthermore, JP-A-9-321157 (Reference 2) discloses split gate type memory cells and proposes a method of elevating hot electron generation and injection efficiencies during the programming by making larger an overlapping between the diffusion layers and the floating gates, making higher the voltage of the diffusion layers than that of the floating gates and also applying a low voltage to the word lines.

Furthermore, Technical Digest of International Electron Devices Meeting (1989), pp 603-606 (Reference 3) discusses a method of controlling the voltage of floating gates and also controlling split channels by third gates other than the floating gates and control gates.

However, the present inventors have found that in the aforementioned memory cells there are several problems in case of highly integrated circuits. The following problems have been found by the present inventors, but the finding has been so far not particularly disclosed yet.

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According to the art disclosed in Reference 1, the memory cells are in such a structure that the upper surfaces of third gates are made higher than the upper surfaces of floating gates. In such memory cell structure, the convex parts at the upper ends of floating gates are counterposed to the third gates through an interlayer dielectric film. When a voltage is applied to the third gates in this structure to conduct an erasing operation, the electric field of the interlayer dielectric film at the upper surfaces of the floating gates is locally enhanced to allow a tunnel current mainly therethrough. Thus, when the erasing operation is carried out in cycles, the interlayer dielectric film around the upper surfaces of the floating gates will be degraded and the charge injected in the floating gates will be leaked to the third gates, rendering retention of data difficult. Electrons are trapped in the interlayer dielectric film around the upper surfaces of the floating gates during cyclic erasing operation, thereby reducing the tunnel current and lowering the erasing speed.

The memory cells disclosed in Reference 1 are in a split channel type memory cell structure devoid of floating gates in parts of the channel regions. The split channels of the memory cells are controlled by controlling a control gate (word line) voltage on the split channels. Thus, the word lines have a split gate function. In programming data into the memory cells,

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it is necessary to elevate the hot electron generation and injection efficiencies. That is, it is effective for this purpose to increase the floating gate voltage, thereby extending the electric field in the vertical direction of the channel regions and lower the split gate voltage, thereby extending the electric field in the horizontal direction of the channel regions. However, in the memory cells disclosed in Reference 1, the split gate voltage is controlled by word line voltage, and thus the floating gate voltage and the split gate voltage cannot be independently controlled. That is, both floating gate voltage and split gate voltage must be controlled by the word line voltage and the electron generation and injection efficiencies cannot be elevated at the same time. Thus, in data programming, a very large quantity of channel current flows, as compared with the injection current, and no simultaneous programming of a plurality of memory cells can be carried out, resulting in failure to attain a high programming speed.

The aforementioned Reference 2 proposes a method of elevating the hot electron generation and injection efficiencies at the same time in the split channel type memory cells, but the proposed method has such a problem that overlapping between the diffusion layer and the floating gates is difficult to obtain due to reduction of memory cell size.

Furthermore, the aforementioned Reference 3

proposes a method of controlling the floating gate voltage by word lines and controlling the split channel by third gates other than the floating gates and control gates, but the proposed method does not take
5 into consideration any issues on the reduction of memory cell size.

Disclosure of Invention

An object of the present invention is to provide a semiconductor integrated circuit device with
10 a reliability improvement and higher programming/erasing speed and a process for producing the same.

The object, and other objects and novel features of the present invention will be apparent from
15 the disclosure of the present specification which follows and the accompanying drawings.

Among the inventions to be disclosed herein, typical embodiments of the invention will be briefly summarized as follows.

20 A process for producing a semiconductor integrated circuit device according to the present invention comprises steps of forming, for example, a p-type (first conduction type) well in a silicon substrate; forming a floating gate pattern (first
25 pattern) through a first insulator film; further forming n-type semiconductor regions to act as sources/drains, forming a second insulator film covering the

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first pattern, forming third gates in gaps formed in the first pattern and further forming control gates, where the height of the upper surfaces of the third gates thus formed is made lower than the upper surface
5 of the first pattern.

Third gates can be formed by any one of a first method of forming a polysilicon film to completely fill the gaps and then dry etching the polysilicon film, a second method of forming a
10 polysilicon film to completely fill the gaps and the polishing the polysilicon film by chemical mechanical polishing (CMP) followed by dry etching, and a third method of forming a polysilicon film to completely fill the gaps, then polishing the polycrystalline film by
15 CMP, then oxidizing the surface of the polysilicon film and selectively removing the oxidized parts.

The third gates can be also formed by any one of a fourth method of forming a polysilicon film so as not to completely fill the gaps, then forming a photo
20 resist film to fill the gaps and dry etching the photo resist film, a fifth method of forming a polysilicon film so as not to completely fill the gaps, then polishing the polysilicon film by CMP, forming a photo resist film to fill the gaps and dry etching the photo
25 resist film and the polysilicon film and a sixth method of forming a polysilicon film so as not to completely fill the gaps, then depositing a silicon oxide film to fill the gaps, polishing the silicon oxide film and the

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polysilicon film by CMP, selectively removing the silicon oxide film in the gaps, forming a photo resist film to fill the gaps and dry etching the photo resist film and the polysilicon film.

5 In the fourth to sixth methods, etching conditions can be so selected that the photo resist film and the polysilicon film can be etched at substantially equal etching speeds.

10 The third gates can be also formed by a seventh method of forming a polysilicon film so as not to completely fill the gaps, then forming a silicon oxide film on the polysilicon film, polishing the silicon oxide film and the polysilicon film by CMP, dry etching the polysilicon film and removing the silicon
15 oxide film.

 In the fourth to seventh methods, the thickness of the polysilicon film can be made smaller than that of the first pattern to act as floating gates.

20 Furthermore, a process according to the present invention comprises forming, for example, a p-type (first conduction type) well in a silicon substrate, forming third gates on the silicon substrate, through a second insulator film, forming n-
25 type (second conduction type) semiconductor regions to act as sources/drains in the well, forming a first insulator film covering the third gates, forming a first pattern to act as floating gates in gaps formed

between the third gates, and further forming control gates, where the height of the upper surface of the third gate is made lower than that of the upper surface of the first pattern to act as the floating gates.

5 The first pattern can be formed by any one of a first method of forming a polysilicon film to completely fill the gaps and then dry etching the polysilicon film, a second method of forming a polysilicon film to completely fill the gaps and then
10 polishing the polysilicon film by CMP, followed by dry etching, a third method of forming a polysilicon film so as not to completely the gaps and then polishing the polysilicon film by CMP, a fourth method of forming a polysilicon film so as not to fill the gaps, then
15 forming a photo resist film to fill the gaps and dry etching the photo resist film and the polysilicon film, and a fifth method of forming a polysilicon film so as not to completely fill the gaps, then depositing a silicon oxide film to fill the gaps and polishing the
20 silicon oxide film and the polysilicon film by CMP.

In the foregoing methods, the third gates can be formed as self-aligned to the floating gates, and also the floating gates can be formed as self-aligned to the third gates.

25 A semiconductor integrated circuit device according to the present invention comprises a first conduction type well formed on the main surface of a semiconductor substrate, second conduction type

semiconductor regions formed in the well, first gates formed on the semiconductor substrate through a first insulator film, second gates formed on the first gates through a second insulator film and third gates formed
5 through the first gates and a third insulator film. The third gates being formed to fill gaps formed between the first gates, where the height of the upper surfaces of the third gates is made lower than the height of the upper surfaces the first gates.

10 In that case, the third gates can be formed as gates having a function of controlling erase gates or split channels or as gates having both of these functions.

The third insulator film can be a nitrogen-
15 introduced silicon oxide film.

Brief Description of Drawings

Fig. 1 is a plan view in part showing a semiconductor integrated circuit device according to Embodiment 1 of the present invention.

20 Fig. 2 (a), (b) and (c) are cross-sectional views along lines A-A', B-B' and C-C' in Fig. 1, respectively.

Fig. 3 (a) to (c) cross-sectionally show steps of a process for producing a semiconductor
25 integrated circuit device according to Embodiment 1 of the present invention.

Fig. 4 (a) to (d) cross-sectionally show

further steps of the process for producing a semiconductor integrated circuit device according to Embodiment 1 of the present invention.

Fig. 5 (a) to (e) cross-sectionally show
5 still further steps of the process for producing a semiconductor integrated circuit device according to Embodiment 1 of the present invention.

Fig. 6 is a graph showing relationships
between programming/erasing cycles and threshold
10 voltage when subjected to programming/erasing cycles.

Fig. 7 is a graph showing results of
measuring changes in threshold voltage when left
standing after 10^6 programming/erasing cycles.

Fig. 8 is a graph showing relationships
15 between a difference in height between the upper surfaces of floating gates and the upper surfaces of third gate and a difference in voltage between the control gates and the third gates, when the erasing operation is about to be completed after predetermined
20 time.

Fig. 9 (a) - (c) cross-sectionally show steps
of a process for producing a semiconductor integrated circuit according to Embodiment 2 of the present invention.

25 Fig. 10 (a) - (d) cross-sectionally show steps of a process for producing a semiconductor integrated circuit device according to Embodiment 3 of the present invention.

Fig. 11 (a) and (b) cross-sectionally show steps of another process for producing a semiconductor integrated circuit device according to Embodiment 3 of the present invention.

5 Fig. 12 (a) - (c) cross-sectionally show steps of a process for producing a semiconductor integrated circuit device according to Embodiment 4 of the present invention.

10 Fig. 13 (a) and (b) cross-sectionally show further steps of a process for producing a semiconductor integrated circuit device according to Embodiment 4 of the present invention, and Fig. 13 (c) is a partially enlarged cross-sectional view around C in Fig. 13 (b), and Fig. 13 (d) is an enlarged view for
15 comparison.

Fig. 14 (a) - (c) cross-sectionally show steps of another process for producing a semiconductor integrated circuit device according to Embodiment 4 of the present invention.

20 Fig. 15 (a) - (c) cross-sectionally show steps of a process for producing a semiconductor integrated circuit device according to Embodiment 5 of the present invention.

Fig. 16 (a) - (c) cross-sectionally show
25 steps of a process for producing a semiconductor integrated circuit device according to Embodiment 6 of the present invention.

Fig. 17 (a) and (b) cross-sectionally show

further steps of a process for producing a semiconductor integrated circuit device according to Embodiment 6 of the present invention.

Fig. 18 (a) - (d) cross-sectionally show
5 steps of a process for producing a semiconductor integrated circuit device according to Embodiment 7 of the present invention.

Fig. 19 (a) - (d) cross-sectionally show
further steps of a process for producing a
10 semiconductor integrated circuit device according to Embodiment 7 of the present invention.

Fig. 20 (a) - (c) cross-sectionally show
still further steps of a process for producing a semiconductor integrated circuit device according to
15 Embodiment 7 of the present invention.

Fig. 21 (a) - (d) cross-sectionally show
steps of a process for producing a semiconductor integrated circuit device according to Embodiment 8 of the present invention.

20 Fig. 22 (a) - (d) cross-sectionally show
steps of a process for producing a semiconductor integrated circuit device according to Embodiment 9 of the present invention.

Fig. 23 (a) - (c) cross-sectionally show
25 further steps of a process for producing a semiconductor integrated circuit device according to Embodiment 9 of the present invention.

Fig. 24 (a) - (c) cross-sectionally show

still further steps of a process for producing a semiconductor integrated circuit device according to Embodiment 9 of the present invention.

In the foregoing Figs. 1 to 24, principal
5 reference numerals used therein have the following meanings:

- 200, 300 and 400: semiconductor substrate
(silicon substrate)
- 201, 301, and 401: well
- 10 202, 302 and 403: insulator film (gate oxide film)
- 402: isolation film
- 203, 203a, 203b, 209, 209a, 307, 307a, 307b, 308, 308a, 308b, 311, 311a, 404 and 404a: floating gate
15 polysilicon film
- 204 and 204a: silicon nitride film
- 205, 305 and 405: diffusion layer region
- 206, 206a, 216b, 306 and 406: nitrogen-introduced silicon oxide film
- 20 207, 207a, 212, 212a, 214, 214', 214a, 214a', 214b, 216, 216a, 216b, 218, 218a, 218b, 219, 219a, 219b, 303, 303a, 410 and 410a: polysilicon film to act as third gates
- 208, 208a, 217, 217a, 217b, 217c, 220, 304
25 and 304a: silicon oxide film
- 210, 210a, 309, 309a and 408: nitrogen-introduced silicon oxide film
- 211, 211a, 310 and 409: polymetal film

211a, 310a and 409a: word line

Best Mode for Carrying Out the Invention

The present invention will be described in detail below, referring to embodiments of the present invention and drawings.

Throughout all the drawings showing embodiments of the present invention, members having the same functions are denoted by the same reference numerals and their repeated explanation will be omitted below.

Embodiment 1

Fig. 1 is a plan view in part of a semiconductor integrated circuit device according to Embodiment 1 of the present invention, and Fig. 2(a), (b) and (c) are cross-sectional views along lines A-A', B-B' and C-C' in Fig. 1, respectively. For easy understanding of the drawing individual members are hatched in the plan view of Fig. 1 and some members are omitted and not shown.

The semiconductor integrated circuit device according to Embodiment 1 of the present invention has so-called flash memory type memory cells, which comprise source/drain diffusion layers 205 in well 201 formed on the main surface of semiconductor substrate 200, first gates (floating gates) 203b, second gates (control gates) 211a and third gates 207a. Control

gates (second gates) 211a of the respective memory cells are connected to one another in the row direction (direction x) to form word lines WL.

Floating gates (first gates) 203b and well
5 201 are isolated from one another by gate insulator film (first insulator film) 202; floating gates 203b and third gates 207a from one another by an insulator film (third insulator film) 206a; floating gates 203b and word lines (control gates) 211a from one another by
10 an insulator film (second insulator film) 210a; and third gates 207a and word lines 211a from one another by an insulator film 208a.

Source/drain diffusion layers 205 are provided as extended in a vertical direction (direction
15 y) to the direction (direction x) of extended word lines 211a and function as local source lines and local data lines, connecting sources/drains of the memory cells in the column direction (direction y). That is, the semiconductor integrated circuit device according
20 to Embodiment 1 of the present invention is composed of so called contactless type array without contact holes in respective memory cells. Channels are formed in the vertical direction (direction x) to the diffusion layers 205.

25 Two side edges each of third gates 207a are counterposed to two of side edges of the floating gates 203b, which are vertical each to word lines 211a and channels through insulator films 206a, respectively.

Third gates 207a exist as filled in gaps formed between floating gates 203b present in the vertical direction (direction y) to word lines 211a and channels. Furthermore, floating gates 203b exist
5 symmetrically to third gates 207a and third gates 207a exist symmetrically to floating gates 203b.

In Embodiment 1 of the present invention, a pair of diffusion layers 205, which form sources/drains, on the other hand, are at an
10 asymmetrical position to floating gate pattern 203b, and one of the diffusion layers is in an offset structure which does not overlap with the floating gates. In Embodiment 1 of the present invention, some of third gates 207a and diffusion layers 205 overlap
15 with each other, so that channels are formed in the well under third gates 207a in Embodiment 1 of the present invention and thus third gates 207a function not only as erase gates, but also as gates which control channels formed thereunder.

20 That is, in programming, a large positive voltage, e.g. about 12 V, is applied to the control gates, a low voltage, e.g. about 2 V, to the third gates and a voltage of about 5 V to the drains, whereas the sources and the well are maintained at zero (0) V,
25 whereby channels are formed in the well under third gates 207a and hot electrons are generated in channels at edges of the floating gates on the source side and electrons are injected into the floating gates. That

is, third gates 207a function as gates, which control channels formed thereunder. The present memory cells can improve hot electron generation and injection efficiencies, as compared with the conventional NOR type flash memory cells and can conduct programming in regions of small channel current. Thus, parallel programming of a large number of memory cells in order of kilobytes or more can be carried out with an internal voltage supply of same level of current drivability as that of prior art.

In erasing, a large negative voltage, e.g. -13.5 V, is applied to the word lines and a small positive voltage, e.g. 3.5 V, to the third gates, whereby a tunnel current is made to flow from the floating gates to the third gates, and the electrons injected in the floating gates are released. That is, third gates 207a function also as erase gates. In Embodiment 1 of the present invention, the upper surfaces of third gates 207a are positioned below the upper surfaces of floating gates 203b, whereby local increase in the electric field at the upper ends of the floating gates can be prevented during the erasing operation, and degradation of the interlayer dielectric film (insulator film 206a) can be suppressed after programming cycles, thereby assuring the reliability of memory cells.

In this structure, even if there are third gates 207a other than floating gates 203b and control

gates 211a, pitch in the wordline (WL) direction
(direction x) and in the local data line direction
(direction y) can be made twice as large as the minimum
feature size. Thus, the memory cell area can be
5 reduced to minimum $4F^2$ (F: minimum feature size) in a
cross-point type array.

Figs. 3 to 5 cross-sectionally show steps of
a process for producing a semiconductor integrated
circuit device according to Embodiment 1 of the present
10 invention.

At first, p-type (first conduction type) well
201 is formed in semiconductor substrate 200, and then
gate insulator film (first insulator film) 202 is
formed to a thickness at about 12 nm on well 201, for
15 example, by a thermal oxidation [Fig. 3(a)].

Then, phosphorus (P)-doped polysilicon film
203 to act as floating gates 203b and silicon nitride
film 204 are successively deposited thereon [Fig.
3(b)]. Deposition of polysilicon film 203 and silicon
20 nitride film 204 can be carried out, for example, by
CVD (chemical vapor deposition).

Then, said silicon nitride film 204 and
polysilicon film 203 are patterned by lithography and
dry etching. By the patterning, silicon nitride film
25 204 and polysilicon film 203 are made into silicon
nitride films 204a and polysilicon films 203a,
respectively [Fig. 3 (c)]. Silicon nitride films 204a
and polysilicon films 203a are formed in a stripe form

by the patterning so that they are extended in the direction y.

Then, arsenic (As) ions are implanted into well 201 by tilted ion implantation to form diffusion layers 205 to act as sources/drains of memory cells [Fig. 3(d)]. Diffusion layers 205 function as source lines or data lines of memory cells. In the ion implantation, silicon nitride films 204a and polysilicon films 203a function as masks, so that diffusion layers 205 are formed as self-aligned to polysilicon films 203a. Since silicon nitride films 204a and polysilicon films 203a are formed in a stripe form as extended in the direction y, diffusion layers 205 are also formed as extended in the direction y. Since diffusion layers are formed by the tilted ion implantation, implanted ions are shielded by silicon nitride film 204a and polysilicon film 203a and thus diffusion layers 205 are not formed in the entire regions between adjacent polysilicon films 203a. Since the ions are implanted in the tilted direction, diffusion layers 205 are formed also partly under polysilicon films 203a, whereby parts each of third gates 207a and diffusion layers 205 are formed as overlapped with one another, as mentioned before, and thus channels are formed in well 201 under third gates 207a.

Since the members etched in the etching step (i.e. silicon nitride films 204a and polysilicon films

203a) contain neither metal films nor metal compound materials, no metals are dissolved in a cleaning step following the etching step and no dissolved metals redeposit on walls of the etched members. Thus, no
5 metals (impurities) are contained in silicon oxide film 206, which will be explained, referring to the next step, whereby defects of silicon oxide film 206 can be suppressed to minimum and the reliability can be improved.

10 Then, silicon oxide film 206 for isolating floating gates 203b from third gates 207a is formed in the following manner.

At first, the silicon oxide film is deposited to a thickness of about 10.5 nm by LPCVD (low pressure
15 chemical vapor deposition) [Fig. 3(e)]. Then, the silicon oxide film is annealed in an ammonia atmosphere to introduce nitrogen into said silicon oxide film 206. Then, nitrogen-introduced silicon oxide film 206 is subjected to wet oxidation to remove hydrogen
20 introduced into the silicon oxide film by annealing in ammonia.

Silicon oxide film 206 formed in the aforementioned manner has a small charge trapping and high programming/erasing endurance characteristics.
25 That is, if the charge is trapped in silicon oxide film 206, the trapped charges are transferred in a nonbiased state to third gates. The larger the amount of transferred electrons, the higher the possibility to

cause retention degradation. The amount of transferred electrons increase with trap density, and thus when the charge trapping is larger in silicon oxide film 206, probability to cause retention degradation will be increased. However in Embodiment 1 of the present invention, the charge trapping in the film is suppressed, the retention degradation will be suppressed and high programming/erasing endurance characteristics can be obtained. Furthermore, silicon oxide film 206 contains no metal impurities, as already mentioned above.

Then, phosphorus (P)-doped polysilicon film 207 to act as third gates 207a is deposited to completely fill gaps in floating gate pattern 203a [Fig. 4(a)]. The polysilicon film can be deposited, for example, by CVD.

Then, polysilicon film 207 is etched back, for example, by anisotropic dry etching, whereby third gates 207a were formed to a predetermined thickness as retained in the gaps in floating gate pattern 203a [Fig. 4(b)], where the thickness of retained polysilicon film (third gates 207a) following the etch back was made smaller than that of floating gate polysilicon 203a. Reliability of insulator film 206a for isolating floating gate polysilicon 203a from third gates 207a can be improved by forming third gates 207a of smaller thickness in this manner, whereby the retention degradation can be reduced as already

mentioned above.

Then, silicon oxide film 208 is deposited to completely fill the gaps in floating gate pattern 203a [Fig. 4(c)]. Deposition of silicon oxide film is
5 carried out, for example, by CVD.

Then, silicon oxide film 208 is polished, for example by CMP (chemical mechanical polishing) until silicon nitride films 204a are exposed (wherein silicon nitride films 204a and silicon oxide films 206 and 208
10 are made into silicon nitride films 204b, insulator films 206a and silicon oxide films 208a, respectively [Fig. 4(d)]).

Then, silicon nitride films 204b are removed with a hot aqueous phosphoric acid solution to expose
15 the surfaces of polysilicons 203a [Fig. 5(a)]. Then, phosphorus (P)-doped polysilicon film 209 is deposited [Fig. 5(b)] and subjected to anisotropic dry etching (whereby polysilicon film 209 are made into polysilicon films 209a) [Fig. 5(c)]. Polysilicon films 209a are
20 electrically connected to polysilicon 203a, and the polysilicons of those two layers form floating gates. polysilicons 209a are effective for increasing the surface area of floating gates, which results in and also increasing the coupling ratio of memory cells,
25 whereby the internal operating voltage can be reduced during the programming/erasing.

Nitrogen-introduced silicon oxide film (film thickness: about 10.5 nm) 210 for isolating floating

gates from word lines is formed in the same manner as shown in Figs. 3(e) [Fig. 5(d)].

Then, a stacked film of a polysilicon film, a tungsten nitride film and a tungsten film, i.e. so-called a polymetal film, is deposited and patterned by lithography and dry etching to form word lines 211a. The patterning is so carried out that word lines 211a are extended in the direction x, that is, in a vertical direction (direction x) to the direction of extended diffusion layers 205 and third gates 207a (direction y).

Furthermore, silicon oxide film 210 and polysilicon films 209a and 203a are etched to complete floating gates (whereby silicon oxide film 210 is made into 210a and polysilicons 203a and 209a are made into 203b and 209b, respectively) [Fig. 5(e)]. To etch silicon oxide film 210 in the etching step, etching is carried out under such conditions that only the silicon oxide film can be etched, whereas to etch polysilicon films 209a and 203a, etching is carried out under such selective etching conditions that silicon can be etched but no silicon oxide film is etched, where insulator films 208a as silicon oxide films function as an etching stopper, so that no third gates 207a under insulator films 208a are etched. That is, floating gates 203b are sectioned in both directions, i.e. direction x and direction y in the etching step to form island-form floating gates, while maintaining third

gates 207 in a stripe form as extended in the direction Y.

Then, an intermetal dielectric film is formed, and then contact holes are formed and connected with word lines 211a, source/drain diffusion layers 205, well 201 and third gates 207a, followed by deposition of a metal layer and patterning thereof to form wirings, thereby completing memory cells, though not shown in the drawing.

Fig. 6 is a graph showing relationships between programming/erasing cycles and threshold voltage when the memory cells formed in the aforementioned manner are subjected to programming/erasing cycles, and also showing together the data as to the memory cells formed by the art of Reference 1 as prior art for comparison.

In the prior art, the erasing speed is lowered when the programming/erasing cycles exceeds about 10^4 , and the threshold voltage is narrowed presumably for the following reasons.

That is, in the prior art, the upper surfaces of the floating gates would be in a lower position than the upper surfaces of the third gates. When an erase voltage is applied to the third gates in memory cells of such a structure, lines of electric force would be concentrated in convex parts at the upper surfaces of the floating gates, and the electric field of the interlayer dielectric film, which performs insulation

between polysilicon at the convex parts would be increased, as compared with the flat parts of side walls of floating gates. Thus, tunnel current would flow only through the convex parts at the upper
5 surfaces of the floating gates, and as a result the interlayer dielectric film at the parts in contact with the convex parts would be degraded in less programming/erasing cycles and electrons would be trapped. The electric field applied to the interlayer
10 dielectric film would be substantially reduced by such an electron trapping, so that the erasing speed would be lowered and the threshold voltage window would be narrowed.

In the memory cells according to Embodiment 1
15 of the present invention, on the other hand, the threshold voltage window is not substantially changed even after 10^6 programming/erasing cycles, because the convex parts on the upper surfaces of floating gates
209a are in contact with thick oxide films 208a, and
20 electron release takes place at the flat parts on side walls of floating gates 203b in case of erasing.

Fig. 7 is a graph showing results of measuring changes in the threshold voltage when to the memory cells according to Embodiment 1 of the present
25 invention are left standing after 10^6 programming/erasing cycles, and also shows results of prior art as measured in the same manner as already mentioned above.

In the prior art, it can be seen that the threshold voltage is largely lowered with increasing standing time, whereas in Embodiment 1 of the present invention no lowering of threshold voltage is observed, because the interlayer dielectric film between the polysilicon is less degraded in case of the memory cells according to Embodiment 1 of the present invention than in the prior art, and leakage of electrons injected into the floating gates to the third gates is suppressed.

Lower position of the upper surfaces of third gates than the position of the upper surfaces of floating gates is also effective for reduction of operating voltage.

Fig. 8 is a graph showing relationships between a difference in height between the upper surfaces of floating gates and the upper surfaces of third gates and a difference in voltage between the control gates and the third gates, when the erasing operation is about to be completed after predetermined cycles, where the thickness of floating gates is made constant, and a difference in height is made positive when the upper surfaces of third gates are in a higher position than that of the upper surfaces of floating gates, whereas a difference in height is made negative when the upper surfaces of third gates are in a lower position than that of the upper surfaces of floating gates. It can be seen from Fig. 8 that the voltage

between the third gates and the control gates can be lowered and the more the operating voltage can be reduced by the lower the position of the upper surfaces of third gates than that of the upper surfaces of floating gates.

When the upper surfaces of third gates are in a higher position than that of the upper surfaces of floating gates, short circuit takes place between the word lines and the third gates, resulting in occurrence of such a failure of conducting desired memory cell operation, and such a failure can be suppressed by bringing the upper surfaces of third gates into a lower position than that of the upper surfaces of floating gates.

Though the memory cells formed in the foregoing manner have third gates other than floating gates and control gates, the dimensions in the direction of local data lines and in the direction of word lines can be made twice as large as their respective minimum feature sizes F , and thus the memory cell area can be reduced to $4F^2$.

Embodiment 2

Fig. 9 cross-sectionally shows steps of a process for producing a semiconductor integrated circuit device according Embodiment 2 of the present invention. Differences of the process according to Embodiment 2 from that of Embodiment 1 are in lower

thickness of deposited polysilicon film to act as third gates than that of Embodiment 1, and coating of a photo resist onto the deposited polysilicon to fill the gaps in the floating gate pattern formed after the polysilicon film deposition, followed by etching back the photo resist and the polysilicon to act as third gates at approximately equal speeds, thereby leaving only polysilicon in the gaps in the floating gate pattern. Arrangement of flash memory cells in plan view, cross-sectional view of completed device and working system are the same as in Embodiment 1 and thus their explanation will be omitted below.

A process according to Embodiment 2 of the present invention will be described below. At first, well 201, gate oxide film 203, floating gate patterns 203a and 204a, diffusion layers 205 and nitrogen-introduced silicon oxide film 206 for isolating floating gates from third gates are successively formed on silicon substrate 200 in the same manner as shown in Fig. 3(a) - (e) of Embodiment 1 (not shown in drawing).

Then, phosphorus-doped polysilicon film 212 to act as third gates is deposited thereon so as not to fill the gaps in floating gate patterns 203a and 204a [Fig. 9(a)]. Thickness of polysilicon film 212 can be made to correspond approximately to thickness of third gates after completion of memory cells.

Then, photo resist 213 is coated thereon to completely fill the gaps in floating gate patterns 203a

and 204a [Fig. 9(b)]. Then, said photo resist 213 and polysilicon film 212 are etched back at approximately equal speeds to leave only polysilicon film 212 to a predetermined thickness in the gaps in floating gate patterns 203a and 204a (whereby polysilicon 212 is made into 212a) [Fig. 9(c)]. Time required for the complete removal of the photo resist is defined as an etching end point.

Then, silicon oxide films 208a, floating gate polysilicon films 209a as a second layer, nitrogen-introduced silicon oxide film 210 and word lines 211a made from a polymetal film are formed thereon in the same manner as in Fig. 4(c) to Fig. 5(e) of Embodiment 1 to complete memory cells.

Memory cells formed in the foregoing manner can reduce fluctuation in thickness of third gaps 212a, as compared with Embodiment 1. That is, polysilicon film 212 is formed as a film and thickness of the film can be made to correspond to thickness of third gates, making it easier to control the film thickness. In Embodiment 2 of the present invention, photo resist 213 with good fluidity is coated, and thus the surface flatness of photo resist 213 at the time of etch-back starting can be improved, resulting in improved flatness of third gates after the etch-back.

Furthermore, in Embodiment 2 of the present invention, end point monitoring of etch-back can be more easily carried out by monitoring a plasma emission intensity

from photo resist 213, resulting in easier control of thickness of third gates. Furthermore, in Embodiment 2 of the present invention, use of photo resist 213 eliminates void formation in the gaps, resulting in improved etch-back controllability and easier thickness control of third gates. In Embodiment 1, on the other hand, the third gates are formed by etch-back in time control, and thus the thickness control is more difficult to conduct than in Embodiment 2 of the present invention. Thus, in Embodiment 2 fluctuation in coupling ratio between memory cells can be reduced and programming/erasing time can be made uniform.

As in Embodiment 1, narrowing of threshold voltage window can be suppressed during the programming/erasing in Embodiment 2, as compared with the prior art. Furthermore, changes in threshold voltage after standing can be suppressed, and operation can be carried out with a lower voltage. Occurrence of short circuit between the erase gates and floating gates can be also suppressed and memory cell area can be reduced to $4F^2$. Furthermore, program size and programming speed can be increased.

Embodiment 3

Fig. 10 cross-sectionally shows steps of a process for producing a semiconductor integrated circuit device according to Embodiment 3 of the present invention. A difference of the process according to

Embodiment 3 of the present invention from that of Embodiment 2 is in removal of polysilicon film on the floating gate patterns by CMP (chemical mechanical polishing) after deposition of the polysilicon film to
5 act as third gates and before photo resist coating and etch-back. Arrangement of flash memory cells in plan view, cross-sectional structure of completed device and working system are the same as in Embodiment 1 and thus their explanation will be omitted below.

10 A process for producing the present memory cells is as follow. Well 201, gate oxide film 202, floating gate patterns 203a and 204a, diffusion layer 205 and nitrogen-introduced silicon oxide film 206 for isolating floating gates from third gates are
15 successively formed on silicon substrate 200 in the same manner as shown in Fig. 3(a) - (e) of Embodiment 1 (not shown in drawing).

Then, phosphorus-doped polysilicon film 214 to act as third gates is deposited thereon so as not to
20 fill the gaps in floating gate patterns 203a and 204a [Fig. 10(a)]. Thickness of polysilicon film 214 is made to correspond approximately to thickness of third gates of completed memory cells.

Then, said polysilicon film 214 is removed by
25 polishing, i.e. by CMP until silicon nitride films 204a of floating gate pattern are exposed (whereby polysilicon film 214 and silicon oxide film 206 are made into 214a and 206a, respectively) [Fig. 10(b)].

Then, photo resist 215 is coated thereon to completely fill the gaps in floating gate patterns 203a and 204a [Fig. 10(c)]. Then, said photo resist 215 and polysilicon films 214a are etched back at approximately equal speeds to leave only polysilicon films 214a to a predetermined thickness in the gaps of floating gate patterns 203 and 204a (whereby polysilicon films 214a are made into 214b) [Fig. 10(a)]. Time required for complete removal of the photo resist is defined as an etching end point.

Then, silicon oxide films 208a, floating gate polysilicon films 209 as a second layer, nitrogen-introduced silicon oxide film 210 and word lines 211a made from a polymetal film are formed thereon in the same manner as shown in Fig. 4(c) - Fig. 5(e) of Embodiment 1 to complete memory cells.

The memory cells formed in the foregoing manner can much more reduce fluctuation in thickness of third gates 214b than in Embodiment 2. That is, in Embodiment 3, the upper surface of polysilicon film 214 is polished by CMP in advance, and thus an etching amount of polysilicon can be reduced, and as a result thickness of third gates 214b can be made smaller. That is, fluctuation in coupling ratio between the memory cells can be made lower, and programming/erasing time can be made uniform.

As in Embodiment 1, narrowing of threshold voltage window can be suppressed during the programming

in Embodiment 3, as compared with the prior art. Furthermore, changes in threshold voltage after standing can be suppressed and operation can be carried out with a lower voltage. Occurrence of short circuit
 5 between the erase gates and the floating gates can be also suppressed and memory cell area can be reduced to $4F^2$. Furthermore, program size and programming speed can be increased.

As shown in Fig. 11, silicon oxide film 214' (e.g. a TEOS oxide film, an SOG film, etc.) can be
 10 formed before polishing polysilicon film 214 by CMP [Fig. 11(a)], and said silicon oxide film 214' and polysilicon film 214 can be polished together by CMP (whereby silicon oxide film 214' is made into 214a')
 15 [Fig. 11(b)]. In that case, polysilicon film 214 never falls down inwardly into the gaps and is never damaged. Then, silicon oxide films 214a' are selectively removed, followed by steps of Fig. 10(b) et seq.

Embodiment 4

20 Figs. 12 and 13 cross-sectionally show steps of a process for producing a semiconductor integrated circuit device according to Embodiment 4 of the present invention. A difference of the process of Embodiment 4 from that of Embodiment 2 is in formation of a silicon
 25 oxide film after deposition of a polysilicon film to act as third gates and its use as a protection film for etch-back. Arrangement of flash memory cells in plan

view, cross-sectional structure of completed device and working system are the same as in Embodiment 1 and thus their explanation will be omitted below.

At first, well 201, gate oxide film 202,
5 floating gate patterns 203a and 204a, diffusion layers 205 and nitrogen-introduced silicon oxide film 206 for isolating floating gates from third gates are successively formed on silicon substrate 200 in the same manner as shown in Fig. 3(a) - (e) of Embodiment 1
10 (not shown in drawing).

Then, phosphorus-doped polysilicon film 216 to act as third gates is deposited thereon so as not to completely fill the gaps in floating gate patterns 203a and 204a [Fig. 12(a)]. Thickness of polysilicon film
15 216 is made approximately to correspond to the thickness of third gates of completed memory cells.

Then, silicon oxide film 217 to act as a protection film when polysilicon film 216 is to be etched back is formed thereon [Fig. 12(b)].

20 Then, said polysilicon film 216 and silicon oxide film 217 are removed by polishing, i.e. CMP, until silicon nitride films 204a of floating gate pattern are exposed (whereby polysilicon film 216, and silicon oxide films 206 and 217 are made into 216a, 206a and 217a, respectively) [Fig. 12(c)].
25

Then, polysilicon films 216a is etched back to leave polysilicon films 216a to a predetermined thickness in the gaps in floating gate patterns 203a

and 204a (whereby polysilicon 216a are made into 216b)
[Fig. 13(a)].

Then, silicon oxide films 217a retained in
the gaps in floating gate patterns 203a and 204a are
5 removed by wet etching [Fig. 13(b)].

Then, silicon oxide films 208a, floating gate
polysilicon films 209a as a second layer, nitrogen-
introduced silicon oxide film 210 and word lines 211a
made from a polymetal film are formed in the same
10 manner as shown in Fig. 4(c) - Fig. 5(e) of Embodiment
1 to complete memory cells.

As in Embodiments 1 to 3, memory cells formed
in Embodiment 4 can suppress narrowing of threshold
voltage window during the programming, as compared with
15 the prior art. Furthermore, changes in threshold
voltage after standing can be suppressed and operation
can be carried out with a lower voltage. Occurrence of
short circuit between the erase gates and the floating
gates can be also suppressed and memory cell area can
20 be reduced to $4F^2$. Furthermore, program size and
programming speed can be increased.

In Embodiment 4, since silicon oxide films
217a are formed in the central regions where third
gates 216b are in a finished state, side wall regions
25 of silicon oxide films 217a, as not covered silicon
oxide films 217a (both end regions of third gates 216b)
are selectively etched. Thus, cross-section of both
etched end regions can be made into a sufficiently flat

shape even in the side wall regions in the finished state of third gates 216b [Fig. 13(c)]. That is, the etching speed of the side wall regions is lower in the ordinary etching, and thus the side wall regions are
5 etched into a shape with sharp projection P in the side wall regions [Fig. 13(d)].

In Embodiment 4, silicon oxide films 217a to act as a mask are formed in the central regions, as already mentioned before, no such shape is formed.
10 Thus, the height of third gates 216b can be surely made lower than that of floating gates 203a, and the object of the present invention can be attained successfully.

As shown in Fig. 14, thick silicon oxide films 217c may be formed to fill the gaps in place of
15 silicon oxide film 217 [Fig. 14(a)]. Then, silicon oxide film 217c and polysilicon film 216 are polished by CMP [Fig. 14(b)], whereby silicon oxide film 217c is made into silicon oxide films 217d, and polysilicon film 216 is made into polysilicon films 216a). Then,
20 polysilicon films 216a are etched back in the same manner as mentioned above, to leave polysilicon films 216a to a predetermined thickness in the gaps in floating gate patterns 203a and 204a (whereby polysilicon films 217d are made into 216b) [Fig.
25 14(c)]. Then, silicon oxide films 217d are removed, followed by steps of Fig. 13(b) et seq. In that case, falling-down of polysilicon film 216 inwardly into the gaps by CMP and the resulting damages can be prevented.

Embodiment 5

Fig. 15 cross-sectionally shows steps of a process for producing a semiconductor integrated circuit device according to Embodiment 5 of the present invention. In Embodiment 5, chemical mechanical polishing and etching-back by dry etching are used together to process the polysilicon film to act as third gates. Arrangement of flash memory cells in plan view, cross-sectional structure of completed device and working system are the same in Embodiment 1 and thus their explanation will be omitted below.

At first, well 201, gate oxide film 202, floating gate patterns 203a and 204a, diffusion layers 205 and nitrogen-introduced silicon oxide film 206 for isolating floating gates for third gates are successively formed on silicon substrate 200 in the same manner as shown in Fig. 3(a) - (e) of Embodiment 1 (not shown in drawing).

Then, phosphorus-doped polysilicon film 218 to act as third gates is deposited thereon to completely fill the gaps in floating gate patterns 203a and 204a [Fig. 15(a)].

Then, said polysilicon film 218 is removed by polishing, i.e. CMP, until silicon nitride film 204a of floating gate pattern are exposed (whereby polysilicon film 218 and silicon oxide film 206 are made into 218a and 206a, respectively) [Fig. 15(b)].

Then, polysilicon films 218a are etched back

to leave polysilicon films 218a to a predetermined thickness in the gaps in floating gate patterns 203a and 204a (whereby polysilicons 218a are made into 218b) [Fig. 15(c)].

5 Then, silicon oxide films 208a, floating gate polysilicon films 209a as a second layer, nitrogen-introduced silicon oxide film 210 and word lines 211a made from a polymetal film are successively formed thereon in the same manner as in Figs. 4(c) to Fig. 10 5(e) of Embodiment 1 to complete memory cells.

As in Embodiments 1 to 4, memory cells formed in Embodiment 5 can suppress narrowing of threshold voltage window during the programming, as compared with the prior art. Furthermore, changes in threshold 15 voltage after standing can be suppressed and operation can be carried out with a lower voltage. Occurrence of short circuit between the third gates and the floating gates can be also suppressed and memory cell area can be reduced to $4F^2$. Furthermore program size and 20 programming speed can be increased.

In the process of Embodiment 5, polysilicon film 218 is polished as shown in Fig. 15(b), and thus the surface is flattened. An amount of polysilicon to be removed by successive etching-back can be reduced 25 and thus load in the etching-back step can be reduced. Furthermore, etching is carried out after the flattening, and thus the surface of polysilicon films 218b can be easily made flat.

Embodiment 6

Figs. 16 and 17 cross-sectionally show steps of a process for producing a semiconductor integrated circuit device according to Embodiment 6 of the present invention. Difference of Embodiment 6 from Embodiments 1-5 is in adjustment of the height of the upper surface of polysilicon film to act as third gates by thermal oxidation. Arrangement of flash memory cells in plan view, cross-sectional structure of completed device and working system are the same as in Embodiment 1 and thus their explanation will be omitted below.

At first, well 201, gate oxide film 202, floating gate patterns 203a and 204a, diffusion layers 205 and nitrogen-introduced silicon oxide film 206 for isolating floating gates from third gates are successively formed on silicon substrate 200 in the same manner as shown in Fig. 3(a) - (e) of Embodiment 1 (not shown in drawing).

Then, phosphorus-doped polysilicon film 219 to act as third gates are deposited thereon to completely fill the gaps in floating gate patterns 203a and 204a [Fig. 16(a)].

Then, polysilicon film 219 is etched back by anisotropic dry etching to leave the film in the gap in floating gate patterns 203a (whereby polysilicon 219 is made into 219a) [Fig. 16(b)].

Then, silicon oxide film 220 is formed on the surfaces of polysilicon films 219a by thermal oxidation

to bring the upper surfaces of polysilicons 219a into a desired position lower than floating gate polysilicon 203a (whereby polysilicon 219a are made into 219b) [Fig. 16(c)], where nitrogen in silicon oxide film 206 is advantageously effective for suppressing oxidation of side walls of floating gate polysilicon 203a.

Then, silicon oxide film 206 present on the upper surfaces of silicon nitride film patterns 204a is removed by an aqueous hydrofluoric acid solution (whereby silicon oxide film is made into 206b) [Fig. 17(a)].

Then, silicon nitride films 204 are removed by a hot aqueous phosphoric acid solution to expose the surfaces of polysilicons 203a [Fig. 17(b)].

The successive steps are the same as those of Fig. 5(b) et seq. of Embodiment 1.

In Embodiment 6, fluctuation in thickness of third gates 219b can be reduced, as compared with Embodiments 1 to 5. That is, in the etch-back step of Fig. 16(b), the surfaces of polysilicon films 219a formed in the gaps between the floating gates can be obtained in a relatively shallow position, and thus can be made flat. Furthermore, silicon oxide film 220 is formed by thermal oxidation, and thus its thickness control can be made more easily. Thus, third gates 219b can be formed under good controllability, so that function in the thickness can be controlled. As a result, fluctuation in coupling ratio between the

memory cells can be reduced and programming/erasing time can be made uniform.

As in Embodiment 1, narrowing of threshold voltage window can be suppressed during the programming in Embodiment 6, as compared with the prior art. Furthermore, changes in threshold voltage after standing can be suppressed and operation can be carried out with a lower voltage. Occurrence of short circuit between the erase gates and the floating gates can be also suppressed and memory cell area can be reduced to $4F^2$. Furthermore, program size and programming speed can be increased.

Embodiment 7

Figs. 18-20 cross-sectionally show steps of a process for producing a semiconductor integrated circuit device according to Embodiment 7 of the present invention. Different from Embodiments 1 to 6, Embodiment 7 shows a case of forming third gates before formation of floating gate patterns. Arrangement of flash memory cells in plan view, and working system are the same as in Embodiment 1 and thus their explanation will be omitted below.

At first, p-type well 301 is formed in silicon substrate 300 and then gate oxide film 302 is formed thereon to a thickness of about 12 nm, for example, by thermal oxidation [Fig. 18(a)].

Then, phosphorus-doped polysilicon film 303

and silicon oxide film to act as third gates are successively deposited thereon [Fig. 18(b)].

Then, said silicon oxide film 304 and polysilicon film 303 are patterned by lithography and dry etching (whereby silicon oxide film and polysilicon film are made into 304a and 303a, respectively) [Fig. 18(c)].

Then, arsenic ions are implanted by tilted ion implantation to form diffusion layers 305 to act as source/drains of memory cells [Fig. 18(d)].

Then, nitrogen-introduced silicon oxide film 306 for isolating floating gates from third gates is formed in the same manner as in Fig. 3(e) of Embodiment 1 [Fig. 19(a)], and phosphorus-doped polysilicon film 307 to act as floating gates is deposited to completely fill the gaps in third gate patterns 303a and 304a [Fig. 19(b)].

Then, polysilicon film 307 is etched back by anisotropic dry etching to leave it in the gaps in third gate patterns 303a and 304a (whereby polysilicon 307 is made into 307a), where an etching amount is so adjusted that the surfaces of polysilicon films 307a are in a higher position than that of the surfaces of polysilicon films 303a [Fig. 19(c)].

Then, phosphorus-doped polysilicon film 308 is deposited thereon [Fig. 19(d)] and then subjected to anisotropic dry etching (whereby polysilicon film 308 is made into 308a) [Fig. 20(a)]. Said polysilicon

films 308a are electrically connected to polysilicons 307a, and two layers of these polysilicons form floating gates. Polysilicons 308a are effective for increasing the floating gate surface area and also
5 increasing coupling ratio of memory cells, whereby internal operating voltage during programming/erasing can be reduced.

Then, nitrogen-introduced silicon oxide film 309 for isolating floating gates from word lines is
10 formed thereon to a thickness of 10.5 nm in the same manner as shown in Fig. 3(e) [Fig. 20(b)].

Then, so called polymetal film 310, i.e. a stacked film of a polysilicon film, a tungsten nitride film and a tungsten film, is deposited thereon and
15 patterned by well known lithography and dry etching to form word lines (whereby polymetal film 310 is made into 310a). Furthermore, silicon oxide film 309, and polysilicon films 308a and 307a are successively etched to complete floating gates (whereby polysilicons 308a
20 and 307a are made into 308b and 307b, respectively, and silicon oxide film 309 into 309a) [Fig. 20(c)].

Then, after formation of an intermetal dielectric film, contact holes in communication with word lines 310a, source/drain diffusion layers 305,
25 well 301 and third gates 303a are formed and then a metal film is deposited thereon and patterned to form wirings, thereby completing memory cells, though not shown in drawing.

In memory cells formed according to Embodiment 7, fluctuation in programming/erasing time between bits can be reduced, as compared with Embodiments 1 to 6, because in Embodiment 7 the position of upper surfaces of third gates depends on deposited film thickness of polysilicon film, and thus fluctuation in coupling ratio between the memory cells can be reduced.

Furthermore, filling of the gaps between floating gate patterns 203a by silicon oxide film 208 and flattening by CMP of Embodiments 1 to 5 are not required in Embodiment 7, simplifying process steps.

As in other Embodiments, narrowing of threshold voltage window can be suppressed during the programming in Embodiment 7, as compared with the prior art. Furthermore, changes in threshold voltage after standing can be suppressed and operation can be carried out with a lower voltage. Occurrence of short circuit between the third gates and the floating gates can be also suppressed and memory cell area can be reduced to $4F^2$. Furthermore, program size and programming speed can be increased.

Embodiment 8

Fig. 21 cross-sectionally shows steps of a process for producing a semiconductor integrated circuit device according to Embodiment 8 of the present invention. The process of Embodiment 8 shows another

case of forming third gates before forming a floating gate pattern. Arrangement of flash memory cells in plan view and working system are the same as in Embodiment 1, and thus their explanation will be
5 omitted below.

p-Type well 301, gate oxide film 302, polysilicon films 303a and silicon oxide films 304a are successively formed on silicon substrate 300, and diffusion layers 305 to act as sources/drains of memory
10 cells and nitrogen-introduced silicon oxide film 306 are formed in the same manner as shown in Fig. 18(a) to Fig. 19(a) of Embodiment 7 (not shown in drawing).

Then, phosphorus-doped polysilicon film 311 to act as floating gates is deposited thereon, where,
15 different from Embodiment 7, thickness of polysilicon film 311 is selected so as not to completely fill the gaps in third gate patterns 303a and 304a [Fig. 21(a)].

Then, polysilicon film 311 is removed by polishing, e.g. CMP, until the upper surfaces of
20 silicon oxide films 304a are exposed (whereby polysilicon film 311 are made into 311a, and silicon oxide films 304a and 306 are made into 304b and 306a, respectively) [Fig. 21(b)]. Here, the polishing is exemplified by CMP, but etching-back may be used, or
25 etching-back may be carried out after filling the gaps with a photo resist, or CMP may be carried out by filling the gaps with a silicon oxide film.

Then, nitrogen-introduced silicon oxide film

310 for isolating floating gates from word lines is formed to a thickness of about 10.5 nm in the same manner as shown in Fig. 3(e) [Fig. 21(c)].

Then, so-called polymetal film 310, i.e. a
5 saked film of a polysilicon film, a tungsten nitride film, and a tungsten film, is deposited thereon, and patterned by well known lithography and dry etching to form word lines (whereby polymetal film 310 is made into 310a). Furthermore, silicon oxide film 309 is
10 etched to complete floating gates (whereby silicon oxide 309 into 309a) [Fig. 21(d)].

Then, after forming an intermetal dielectric film, contact holes in connection with word lines 310a, source/drain diffusion layers 305, well 301 and third
15 gates 303a are formed, and then a metal film is formed and patterned to form wirings, thereby completing memory cells (not shown in drawing).

In memory cells formed according to Embodiment 8, fluctuation in programming/erasing time
20 between bits can be reduced. Since the floating gates are formed from a single layer of polysilicon, the process steps can be more simplified than those of Embodiment 7.

Furthermore, as in other Embodiments,
25 narrowing of threshold voltage window can be suppressed during the programming in Embodiment 8, as compared with the prior art. Furthermore, changes in threshold voltage after standing can be suppressed and operation

can be carried out with a lower voltage. Occurrence of short circuit between the third gates and the floating gates can be also suppressed and memory cell area can be reduced to $4F^2$. Furthermore, program size and
5 programming speed can be increased.

Embodiment 9

Figs. 22-24 cross-sectionally show steps of a process for producing a semiconductor integrated circuit device according to Embodiment 9 of the present
10 invention.

At first, p-type well 401 is formed in silicon substrate 400, and field oxide film 402 to act as an isolation region is formed thereon [Fig. 22(a)]. Then, gate oxide film 403 is formed by thermal
15 oxidation [Fig. 22(b)].

Then, phosphorus-doped polysilicon film 404 to act as floating gates are deposited thereon [Fig. 22(c)], and patterned by lithography and dry etching to form floating gates (whereby polysilicon film is made
20 into 404a) [Fig. 22(d)].

Then, arsenic ions are implanted therein by ion implantation to form diffusion layers 405 to act as sources/drains of memory cells (not shown in drawing).

Then, insulator film 405 for isolating
25 floating gates from third gates is formed in the same manner as shown in Fig. 3(e) of Embodiment 1 [Fig. 23(a)].

Then, phosphorus-doped polysilicon film 410 to act as third gates are deposited thereon to completely fill the gaps in floating gate patterns 404a [Fig. 23(b)].

5 Then, polysilicon film 410 is etched back by dry etching so that the upper surface of polysilicon film 410 can be in a lower position than that of upper surfaces of floating gate polysilicons 404a (whereby polysilicon 410 is made into 410a) [Fig. 23(c)].

10 Then, nitrogen-introduced silicon oxide film 408 for isolating floating gates from word lines is formed in the same manner as shown in Fig. 3(e) of Embodiment 1 [Fig. 24(a)].

Then, so called polymetal film 409, i.e. a
15 stacked film of a polysilicon film, a tungsten nitride film and a tungsten film, is deposited thereon [Fig. 24(b)], and then patterned by lithography and dry etching to form word lines (whereby polymetal film 409 is made into 409a) [Fig. 24(c)].

20 Then, after forming an intermetal dielectric film, contact holes in communication with word lines 409a, source/drain diffusion layers 405, well 401 and third gates 407a are formed, and then a metal layer is deposited and patterned to form wirings, thereby
25 completing memory cells (not shown in drawing).

In memory cells formed according to Embodiment 9, narrowing of threshold voltage window can be suppressed during programming/erasing cycles, as

compared with the prior art. Furthermore, changes in threshold voltage after standing can be suppressed and operation can be carried out with a lower voltage.

According to Embodiment 9, reliability of a semiconductor integrated circuit device after programming/erasing cycles can be effectively improved and internal operating voltage can be effectively reduced.

In the foregoing, the present invention has been described in detail, referring to Embodiments, but the present invention shall not be limited only to the foregoing Embodiments, but, needless to say, can be variously modified within the spirit and the scope of the present invention.

For example, in the foregoing embodiments, a stacked film of a polysilicon film, a tungsten nitride film and a tungsten film is used as materials for word lines, but even other barrier metal films, e.g. films of a transition metal element itself, such as tungsten, titanium, tantalum, etc., or its nitrides, or its silicides, or an aluminum nitride, a cobalt silicide film, a molybdenum silicide film or alloy films such as a titanium-tungsten film, etc. can be used to obtain equivalent effects in place of the tungsten nitride film. Furthermore, even a stacked film of a polysilicon film and a metal silicide film, i.e. so-called polycide film, can have an equivalent effect. Typical example of the metal silicide film is a

tungsten silicide film. Even a polysilicon monolayer film has an equivalent effect.

In the foregoing Embodiments, a nitrogen-introduced silicon oxide film is used as an insulator film for isolating floating gates from third gates, but when the present non-volatile semiconductor memory device is applied to products of less programming/erasing cycles, a silicon oxide film formed by conventional thermal oxidation or CVD may be used.

In the foregoing Embodiments, a nitrogen-introduced silicon oxide film is also used as an insulator film for isolating floating gates from control gates, but when the device is applied to cases where the internal operating voltage during the programming/ erasing or programming/erasing speed is not so important, a so far widely used stack film of silicon oxide film/silicon nitride film/silicon oxide film, i.e. a so-called ONO film may be used as the insulator film.

In the foregoing Embodiments, description has been made of n-channel type memory cells, in which n-type diffusion layers are formed in p-type well, but p-channel type memory cells, in which the diffusion layers are of p-type, have an equivalent effect. In that case, voltages of control gates, third gates and drains during the programming/erasing will be negative, relative to the well voltage. In that case, electron injection is made by hot electrons.

In the foregoing Embodiments, the third gates have both functions of gates for controlling split channels and of erase gates during the programming/erasing, but may have any one of the functions.

5 Industrial Applicability

In the foregoing Embodiments, necessary levels of electrons injected into floating gates during programming/erasing are minimum two, but the present invention may be applied to so-called multilevel storage of forming at least 4 levels and storing at least 2 bits in one memory cell. In the conventional multilevel storage, there has been a problem of a larger difference between the lowest threshold voltage level and the highest threshold voltage level, as compared with two-level storage, even if the amount of electrons injected into the floating gates is precisely controlled to compress the threshold voltage distribution on the respective levels. Thus, in the Fowler-Nordheim type programming/erasing, there has been such a problem that the programming/erasing speed is retarded or the programming/erasing voltage is increased. In the present invention, programming and erasing can be carried out with a lower voltage such as 13.5 V or lower. In other words, the programming/erasing can be carried out at a higher speed, and thus the present invention is very effective for the multilevel storage system.

Furthermore, the present invention can be widely applied to semiconductor devices provided with a memory cell array having an non-volatile semiconductor memory device, e.g. one-chip microcomputers, system

5 LSI, etc.

Typical effects of the present invention can be summarized as follows: improved reliability of a semiconductor integrated circuit device after programming/erasing cycles; reduced internal operating

10 voltage of a semiconductor integrated circuit device; improved yield of a semiconductor integrated circuit device; reduced memory cell area of a semiconductor integrated circuit device; and improved operating speed of a semiconductor integrated circuit device.

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CLAIMS

1. A process for producing a semiconductor integrated circuit device, which comprises a step of forming a first conduction type well in a silicon substrate; a step of forming a first pattern to act as floating gates on the silicon substrate through a first insulator film; a step of forming second conduction type semiconductor regions to act as sources/drains in the well; a step of forming a second insulator film covering the first pattern; a step of forming third gates in gaps formed in the first pattern through the second insulator film; a step of forming control gates on the upper surfaces of the floating gates and the third gates, the height of the upper surfaces of the third gates formed being lower than the height of the upper surface of the first pattern.

2. A process according to Claim 1, wherein the third gates are formed by any one of a first method of forming a polysilicon film completely filling the gaps, and then dry etching the polysilicon film, a second method of forming a polysilicon film completely filling the gaps, and then polishing the polysilicon film by chemical mechanical polishing, followed by dry etching, and a third method of forming a polysilicon film completely filling the gaps, then polishing the polysilicon film by chemical mechanical polishing, oxidizing the surface of the polysilicon film and selectively removing the oxidized parts.

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3. A process according to Claim 1, wherein the third gates are formed by any one of a first method of forming a polysilicon film so as not to completely fill the gaps, then forming a photo resist film to fill the gap, and dry etching the photo resist film and the polysilicon film, a second method of forming a polysilicon film so as not to completely fill the gaps, then polishing the polysilicon film by chemical mechanical polishing, forming a photo resist to fill the gaps and dry etching the photo resist film and the polysilicon film, and a third method of forming a polysilicon film so as not to completely fill the gaps, then depositing a silicon oxide film to fill the gaps, polishing the silicon oxide film and the polysilicon film by chemical mechanical polishing, selectively removing the silicon oxide film in the gaps, forming a photo resist film to fill the gaps and dry etching the photo resist film and the polysilicon film.

4. A process according to Claim 3, wherein the dry etching of the photo resist and the polysilicon film is carried out at substantially equal etching speeds.

5. A process according to Claim 1, wherein the third gates are formed by a method of forming a polysilicon film so as not to completely fill the gaps, then forming a silicon oxide film on the polysilicon film, polishing the silicon oxide film and the polysilicon film by chemical mechanical polishing, dry

etching the polysilicon film and removing the silicon oxide film.

6. A process according to any one of Claims 3 to 5, wherein the thickness of the polysilicon film is made smaller than that of the first pattern to act as the floating gates.

7. A process for producing a semiconductor integrated circuit device, which comprises a step of forming a first conduction type well in a silicon substrate; a step of forming third gates on the silicon substrate through a second insulator film; a step of forming second conduction type semiconductor regions to act as sources/drains in the well; a step of forming a first insulator film covering the third gates; a step of forming a first pattern to act as floating gates in gaps formed between the third gates through the first insulator film; and a step of forming control gates on the upper surfaces of the floating gates and the third gates, the height of the upper surfaces of the third gates thus formed being made lower than that of the upper surface of the first pattern.

8. A process according to Claim 7, wherein the first pattern is formed by any one of a first method of forming a polysilicon film to completely fill the gaps, and then dry etching the polysilicon film, a second method of forming a polysilicon film to completely fill the gaps and then polishing the polysilicon film by chemical mechanical polishing, followed by dry etching;

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a third method of forming a polysilicon film so as not to completely fill the gaps and then polishing the polysilicon film by chemical mechanical polishing, a fourth method of forming a polysilicon film so as not to completely fill the gaps, then forming a photo resist film to fill the gaps and dry etching the photo resist film and the polysilicon film, and a fifth method of forming a polysilicon film so as not to completely fill the gaps, then depositing a silicon oxide film to fill the gaps and polishing the silicon oxide film and the polysilicon film by chemical mechanical polishing.

9. A process according to any one of Claims 1 to 8, wherein the third gates are self-aligned to the floating gates.

10. A process according to any one of Claims 1 to 8, wherein the floating gates are self-aligned to the third gates.

11. A semiconductor integrated circuit device, which comprises a first conduction type well formed on the main surface of a semiconductor substrate, second conduction type semiconductor regions formed in the well, first gates formed on the semiconductor substrate through a first insulator film, second gates formed on the first gates through a second insulator film and third gates formed through the first gates and a third insulator film, the third gates being formed to fill gaps between the first gates and the height of the

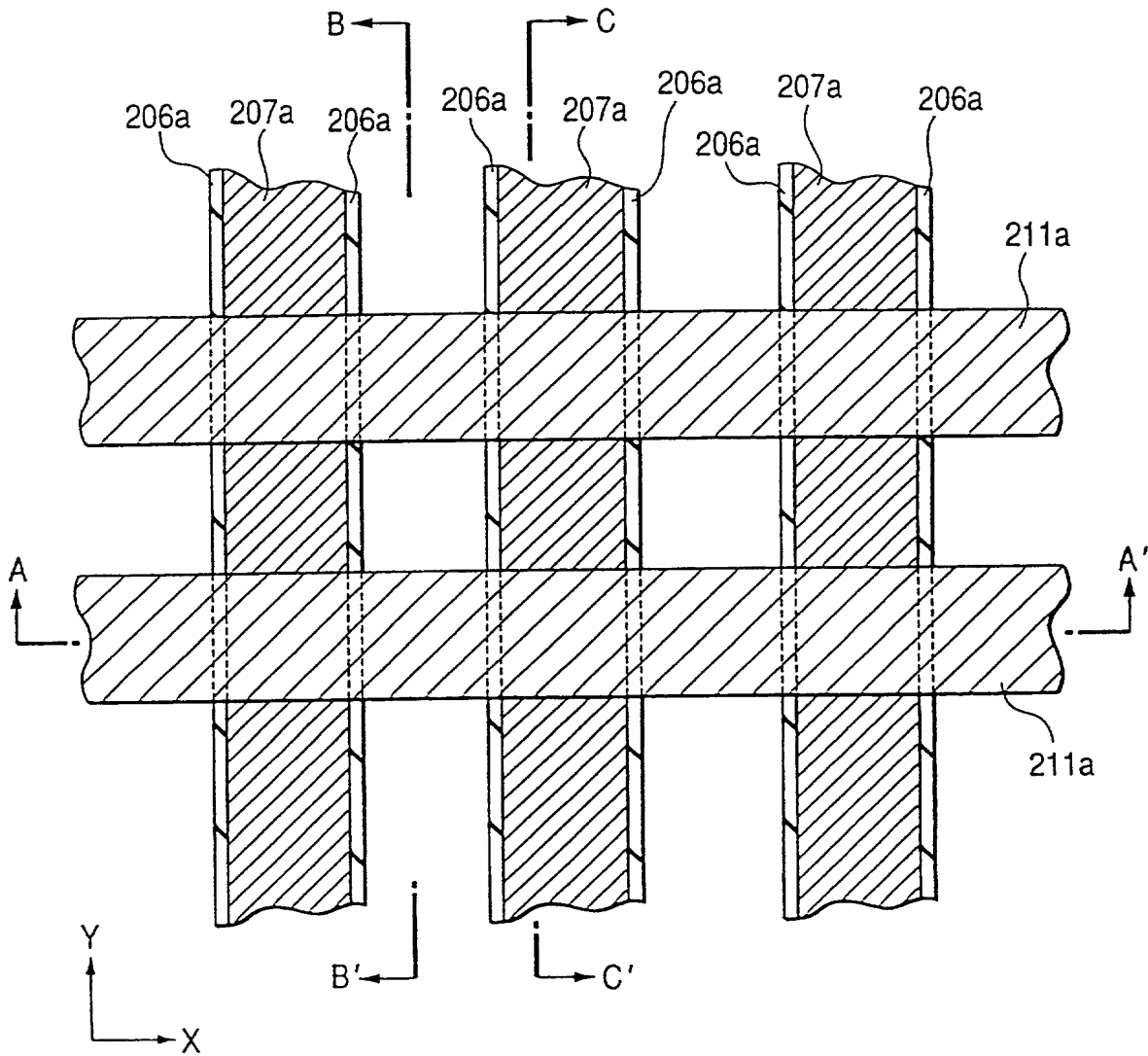
surfaces of the third gates being made lower than that of the surfaces of the first gates.

12. A semiconductor integrated circuit device according to Claim 11, wherein the third gates are in any one of a first structure of erase gates, a second structure of gates controlling split channels, and a third structure having both functions of erase gates and gates controlling split channels.

13. A semiconductor integrated circuit device according to Claim 11 or 12, wherein the third insulator film is a nitrogen-introduced silicon oxide film.

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FIG. 1



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DESCRIPTION

SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND PROCESS FOR PRODUCING THE SAME

Technical Field

The present invention relates to a semiconductor integrated circuit device and a process for producing the same, and particularly to a technique of realizing integration, reliability improvement and low voltage operation at a high speed of a nonvolatile semiconductor memory device capable of electrically programming/erasing.

Background Art

Among nonvolatile semiconductor memory devices capable of electrically programming/erasing, the so-called flash memory capable of bulk erasing is well known. Flash memory is distinguished in mobility and impact resistance and is capable of electrically conducting bulk erasing and thus is now in rapidly increasing demand as the file (memory device) of personal digital assistants such as mobile personal computers, digital still cameras, etc. Reduction in bit cost by reducing the memory cell area is an important factor in the market expansion. For example, as disclosed in Ohyobutsuri, 65, No. 11, 1114-1124, published by Japan Society of Applied Physics (Ohyobutsuri-Gakkai) on November 10, 1996, various

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memory cell systems have been proposed for its realization.

On the other hand, Japanese Patent No. 2,694,618 (Reference 1) discloses a virtual ground type memory cell using three-layered polysilicon gates. That is, the memory cells each comprise a semiconductor region and three kinds of gates formed on a well in a semiconductor substrate. Three kind of gates are a floating gate formed on the well, a control gate formed on the floating gate and an erase gate formed between the adjacent control gate and floating gate. The three kinds of gates are made of polysilicon and isolated from one another by insulator films, respectively, and the floating gate and the well are also isolated from each other by another insulator film. The control gates are connected in the row direction (direction x) to form word lines. Source/drain diffusion layers are formed in the column direction as a virtual ground type, sharing with the adjacent memory cell and diffusion layer to attain pitch reduction in the column direction. The erase gates are arranged in parallel to channels and also in parallel to the word lines and between the word lines (control gates).

In the programming of the memory cells as described in Reference 1, a positive voltage is mutually independently applied to the word lines and the drains, whereas the well, the sources and the erase gates are maintained at zero (0) volt, whereby hot

electrons are generated in the channel regions near the drains, and electrons are injected into the floating gates to elevate the threshold voltage of the memory cells. In the erasing, a positive voltage is applied
5 to the erase gates, whereas the word lines, the sources and the well are maintained at zero (0) V, whereby electrons are emitted from the floating gates to the erase gates to lower the threshold voltage.

Furthermore, JP-A-9-321157 (Reference 2)
10 discloses split gate type memory cells and proposes a method of elevating hot electron generation and injection efficiencies during the programming by making larger an overlapping between the diffusion layers and the floating gates, making higher the voltage of the
15 diffusion layers than that of the floating gates and also applying a low voltage to the word lines.

Furthermore, Technical Digest of
International Electron Devices Meeting (1989), pp 603-606 (Reference 3) discusses a method of controlling the
20 voltage of floating gates and also controlling split channels by third gates other than the floating gates and control gates.

However, the present inventors have found that in the aforementioned memory cells there are
25 several problems in case of highly integrated circuits. The following problems have been found by the present inventors, but the finding has been so far not particularly disclosed yet.

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According to the art disclosed in Reference 1, the memory cells are in such a structure that the upper surfaces of third gates are made higher than the upper surfaces of floating gates. In such memory cell structure, the convex parts at the upper ends of floating gates are counterposed to the third gates through an interlayer dielectric film. When a voltage is applied to the third gates in this structure to conduct an erasing operation, the electric field of the interlayer dielectric film at the upper surfaces of the floating gates is locally enhanced to allow a tunnel current mainly therethrough. Thus, when the erasing operation is carried out in cycles, the interlayer dielectric film around the upper surfaces of the floating gates will be degraded and the charge injected in the floating gates will be leaked to the third gates, rendering retention of data difficult. Electrons are trapped in the interlayer dielectric film around the upper surfaces of the floating gates during cyclic erasing operation, thereby reducing the tunnel current and lowering the erasing speed.

The memory cells disclosed in Reference 1 are in a split channel type memory cell structure devoid of floating gates in parts of the channel regions. The split channels of the memory cells are controlled by controlling a control gate (word line) voltage on the split channels. Thus, the word lines have a split gate function. In programming data into the memory cells,

it is necessary to elevate the hot electron generation and injection efficiencies. That is, it is effective for this purpose to increase the floating gate voltage, thereby extending the electric field in the vertical direction of the channel regions and lower the split gate voltage, thereby extending the electric field in the horizontal direction of the channel regions. However, in the memory cells disclosed in Reference 1, the split gate voltage is controlled by word line voltage, and thus the floating gate voltage and the split gate voltage cannot be independently controlled. That is, both floating gate voltage and split gate voltage must be controlled by the word line voltage and the electron generation and injection efficiencies cannot be elevated at the same time. Thus, in data programming, a very large quantity of channel current flows, as compared with the injection current, and no simultaneous programming of a plurality of memory cells can be carried out, resulting in failure to attain a high programming speed.

The aforementioned Reference 2 proposes a method of elevating the hot electron generation and injection efficiencies at the same time in the split channel type memory cells, but the proposed method has such a problem that overlapping between the diffusion layer and the floating gates is difficult to obtain due to reduction of memory cell size.

Furthermore, the aforementioned Reference 3

proposes a method of controlling the floating gate voltage by word lines and controlling the split channel by third gates other than the floating gates and control gates, but the proposed method does not take
5 into consideration any issues on the reduction of memory cell size.

Disclosure of Invention

An object of the present invention is to provide a semiconductor integrated circuit device with
10 a reliability improvement and higher programming/erasing speed and a process for producing the same.

The object, and other objects and novel features of the present invention will be apparent from
15 the disclosure of the present specification which follows and the accompanying drawings.

Among the inventions to be disclosed herein, typical embodiments of the invention will be briefly summarized as follows.

20 A process for producing a semiconductor integrated circuit device according to the present invention comprises steps of forming, for example, a p-type (first conduction type) well in a silicon substrate; forming a floating gate pattern (first
25 pattern) through a first insulator film; further forming n-type semiconductor regions to act as sources/ drains, forming a second insulator film covering the

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first pattern, forming third gates in gaps formed in the first pattern and further forming control gates, where the height of the upper surfaces of the third gates thus formed is made lower than the upper surface
5 of the first pattern.

Third gates can be formed by any one of a first method of forming a polysilicon film to completely fill the gaps and then dry etching the polysilicon film, a second method of forming a
10 polysilicon film to completely fill the gaps and the polishing the polysilicon film by chemical mechanical polishing (CMP) followed by dry etching, and a third method of forming a polysilicon film to completely fill the gaps, then polishing the polycrystalline film by
15 CMP, then oxidizing the surface of the polysilicon film and selectively removing the oxidized parts.

The third gates can be also formed by any one of a fourth method of forming a polysilicon film so as not to completely fill the gaps, then forming a photo
20 resist film to fill the gaps and dry etching the photo resist film, a fifth method of forming a polysilicon film so as not to completely fill the gaps, then polishing the polysilicon film by CMP, forming a photo resist film to fill the gaps and dry etching the photo
25 resist film and the polysilicon film and a sixth method of forming a polysilicon film so as not to completely fill the gaps, then depositing a silicon oxide film to fill the gaps, polishing the silicon oxide film and the

polysilicon film by CMP, selectively removing the silicon oxide film in the gaps, forming a photo resist film to fill the gaps and dry etching the photo resist film and the polysilicon film.

- 5 In the fourth to sixth methods, etching conditions can be so selected that the photo resist film and the polysilicon film can be etched at substantially equal etching speeds.

- The third gates can be also formed by a
10 seventh method of forming a polysilicon film so as not to completely fill the gaps, then forming a silicon oxide film on the polysilicon film, polishing the silicon oxide film and the polysilicon film by CMP, dry etching the polysilicon film and removing the silicon
15 oxide film.

 In the fourth to seventh methods, the thickness of the polysilicon film can be made smaller than that of the first pattern to act as floating gates.

- 20 Furthermore, a process according to the present invention comprises forming, for example, a p-type (first conduction type) well in a silicon substrate, forming third gates on the silicon substrate, through a second insulator film, forming n-
25 type (second conduction type) semiconductor regions to act as sources/drains in the well, forming a first insulator film covering the third gates, forming a first pattern to act as floating gates in gaps formed

between the third gates, and further forming control gates, where the height of the upper surface of the third gate is made lower than that of the upper surface of the first pattern to act as the floating gates.

5 The first pattern can be formed by any one of a first method of forming a polysilicon film to completely fill the gaps and then dry etching the polysilicon film, a second method of forming a polysilicon film to completely fill the gaps and then
10 polishing the polysilicon film by CMP, followed by dry etching, a third method of forming a polysilicon film so as not to completely the gaps and then polishing the polysilicon film by CMP, a fourth method of forming a polysilicon film so as not to fill the gaps, then
15 forming a photo resist film to fill the gaps and dry etching the photo resist film and the polysilicon film, and a fifth method of forming a polysilicon film so as not to completely fill the gaps, then depositing a silicon oxide film to fill the gaps and polishing the
20 silicon oxide film and the polysilicon film by CMP.

In the foregoing methods, the third gates can be formed as self-aligned to the floating gates, and also the floating gates can be formed as self-aligned to the third gates.

25 A semiconductor integrated circuit device according to the present invention comprises a first conduction type well formed on the main surface of a semiconductor substrate, second conduction type

semiconductor regions formed in the well, first gates formed on the semiconductor substrate through a first insulator film, second gates formed on the first gates through a second insulator film and third gates formed
5 through the first gates and a third insulator film.

The third gates being formed to fill gaps formed between the first gates, where the height of the upper surfaces of the third gates is made lower than the height of the upper surfaces the first gates.

10 In that case, the third gates can be formed as gates having a function of controlling erase gates or split channels or as gates having both of these functions.

The third insulator film can be a nitrogen-
15 introduced silicon oxide film.

Brief Description of Drawings

Fig. 1 is a plan view in part showing a semiconductor integrated circuit device according to Embodiment 1 of the present invention.

20 Fig. 2 (a), (b) and (c) are cross-sectional views along lines A-A', B-B' and C-C' in Fig. 1, respectively.

Fig. 3 (a) to (c) cross-sectionally show steps of a process for producing a semiconductor
25 integrated circuit device according to Embodiment 1 of the present invention.

Fig. 4 (a) to (d) cross-sectionally show

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further steps of the process for producing a semiconductor integrated circuit device according to Embodiment 1 of the present invention.

Fig. 5 (a) to (e) cross-sectionally show
5 still further steps of the process for producing a semiconductor integrated circuit device according to Embodiment 1 of the present invention.

Fig. 6 is a graph showing relationships between programming/erasing cycles and threshold
10 voltage when subjected to programming/erasing cycles.

Fig. 7 is a graph showing results of measuring changes in threshold voltage when left standing after 10^6 programming/erasing cycles.

Fig. 8 is a graph showing relationships
15 between a difference in height between the upper surfaces of floating gates and the upper surfaces of third gate and a difference in voltage between the control gates and the third gates, when the erasing operation is about to be completed after predetermined
20 time.

Fig. 9 (a) - (c) cross-sectionally show steps of a process for producing a semiconductor integrated circuit according to Embodiment 2 of the present invention.

25 Fig. 10 (a) - (d) cross-sectionally show steps of a process for producing a semiconductor integrated circuit device according to Embodiment 3 of the present invention.

Fig. 11 (a) and (b) cross-sectionally show steps of another process for producing a semiconductor integrated circuit device according to Embodiment 3 of the present invention.

5 Fig. 12 (a) - (c) cross-sectionally show steps of a process for producing a semiconductor integrated circuit device according to Embodiment 4 of the present invention.

Fig. 13 (a) and (b) cross-sectionally show
10 further steps of a process for producing a semiconductor integrated circuit device according to Embodiment 4 of the present invention, and Fig. 13 (c) is a partially enlarged cross-sectional view around C in Fig. 13 (b), and Fig. 13 (d) is an enlarged view for
15 comparison.

Fig. 14 (a) - (c) cross-sectionally show steps of another process for producing a semiconductor integrated circuit device according to Embodiment 4 of the present invention.

20 Fig. 15 (a) - (c) cross-sectionally show steps of a process for producing a semiconductor integrated circuit device according to Embodiment 5 of the present invention.

Fig. 16 (a) - (c) cross-sectionally show
25 steps of a process for producing a semiconductor integrated circuit device according to Embodiment 6 of the present invention.

Fig. 17 (a) and (b) cross-sectionally show

further steps of a process for producing a semiconductor integrated circuit device according to Embodiment 6 of the present invention.

Fig. 18 (a) - (d) cross-sectionally show
5 steps of a process for producing a semiconductor integrated circuit device according to Embodiment 7 of the present invention.

Fig. 19 (a) - (d) cross-sectionally show further steps of a process for producing a
10 semiconductor integrated circuit device according to Embodiment 7 of the present invention.

Fig. 20 (a) - (c) cross-sectionally show still further steps of a process for producing a semiconductor integrated circuit device according to
15 Embodiment 7 of the present invention.

Fig. 21 (a) - (d) cross-sectionally show steps of a process for producing a semiconductor integrated circuit device according to Embodiment 8 of the present invention.

20 Fig. 22 (a) - (d) cross-sectionally show steps of a process for producing a semiconductor integrated circuit device according to Embodiment 9 of the present invention.

Fig. 23 (a) - (c) cross-sectionally show
25 further steps of a process for producing a semiconductor integrated circuit device according to Embodiment 9 of the present invention.

Fig. 24 (a) - (c) cross-sectionally show

still further steps of a process for producing a semiconductor integrated circuit device according to Embodiment 9 of the present invention.

In the foregoing Figs. 1 to 24, principal
5 reference numerals used therein have the following meanings:

- 200, 300 and 400: semiconductor substrate
(silicon substrate)
- 201, 301, and 401: well
- 10 202, 302 and 403: insulator film (gate oxide film)
- 402: isolation film
- 203, 203a, 203b, 209, 209a, 307, 307a, 307b, 308, 308a, 308b, 311, 311a, 404 and 404a: floating gate
15 polysilicon film
- 204 and 204a: silicon nitride film
- 205, 305 and 405: diffusion layer region
- 206, 206a, 216b, 306 and 406: nitrogen-introduced silicon oxide film
- 20 207, 207a, 212, 212a, 214, 214', 214a, 214a', 214b, 216, 216a, 216b, 218, 218a, 218b, 219, 219a, 219b, 303, 303a, 410 and 410a: polysilicon film to act as third gates
- 208, 208a, 217, 217a, 217b, 217c, 220, 304
25 and 304a: silicon oxide film
- 210, 210a, 309, 309a and 408: nitrogen-introduced silicon oxide film
- 211, 211a, 310 and 409: polymetal film

211a, 310a and 409a: word line

Best Mode for Carrying Out the Invention

The present invention will be described in detail below, referring to embodiments of the present invention and drawings.

Throughout all the drawings showing embodiments of the present invention, members having the same functions are denoted by the same reference numerals and their repeated explanation will be omitted below.

Embodiment 1

Fig. 1 is a plan view in part of a semiconductor integrated circuit device according to Embodiment 1 of the present invention, and Fig. 2(a), (b) and (c) are cross-sectional views along lines A-A', B-B' and C-C' in Fig. 1, respectively. For easy understanding of the drawing individual members are hatched in the plan view of Fig. 1 and some members are omitted and not shown.

The semiconductor integrated circuit device according to Embodiment 1 of the present invention has so-called flash memory type memory cells, which comprise source/drain diffusion layers 205 in well 201 formed on the main surface of semiconductor substrate 200, first gates (floating gates) 203b, second gates (control gates) 211a and third gates 207a. Control

gates (second gates) 211a of the respective memory cells are connected to one another in the row direction (direction x) to form word lines WL.

Floating gates (first gates) 203b and well 201 are isolated from one another by gate insulator film (first insulator film) 202; floating gates 203b and third gates 207a from one another by an insulator film (third insulator film) 206a; floating gates 203b and word lines (control gates) 211a from one another by an insulator film (second insulator film) 210a; and third gates 207a and word lines 211a from one another by an insulator film 208a.

Source/drain diffusion layers 205 are provided as extended in a vertical direction (direction y) to the direction (direction x) of extended word lines 211a and function as local source lines and local data lines, connecting sources/drains of the memory cells in the column direction (direction y). That is, the semiconductor integrated circuit device according to Embodiment 1 of the present invention is composed of so called contactless type array without contact holes in respective memory cells. Channels are formed in the vertical direction (direction x) to the diffusion layers 205.

Two side edges each of third gates 207a are counterposed to two of side edges of the floating gates 203b, which are vertical each to word lines 211a and channels through insulator films 206a, respectively.

Third gates 207a exist as filled in gaps formed between floating gates 203b present in the vertical direction (direction y) to word lines 211a and channels. Furthermore, floating gates 203b exist
5 symmetrically to third gates 207a and third gates 207a exist symmetrically to floating gates 203b.

In Embodiment 1 of the present invention, a pair of diffusion layers 205, which form sources/drains, on the other hand, are at an
10 asymmetrical position to floating gate pattern 203b, and one of the diffusion layers is in an offset structure which does not overlap with the floating gates. In Embodiment 1 of the present invention, some of third gates 207a and diffusion layers 205 overlap
15 with each other, so that channels are formed in the well under third gates 207a in Embodiment 1 of the present invention and thus third gates 207a function not only as erase gates, but also as gates which control channels formed thereunder.

20 That is, in programming, a large positive voltage, e.g. about 12 V, is applied to the control gates, a low voltage, e.g. about 2 V, to the third gates and a voltage of about 5 V to the drains, whereas the sources and the well are maintained at zero (0) V,
25 whereby channels are formed in the well under third gates 207a and hot electrons are generated in channels at edges of the floating gates on the source side and electrons are injected into the floating gates. That

is, third gates 207a function as gates, which control channels formed thereunder. The present memory cells can improve hot electron generation and injection efficiencies, as compared with the conventional NOR type flash memory cells and can conduct programming in regions of small channel current. Thus, parallel programming of a large number of memory cells in order of kilobytes or more can be carried out with an internal voltage supply of same level of current drivability as that of prior art.

In erasing, a large negative voltage, e.g. -13.5 V, is applied to the word lines and a small positive voltage, e.g. 3.5 V, to the third gates, whereby a tunnel current is made to flow from the floating gates to the third gates, and the electrons injected in the floating gates are released. That is, third gates 207a function also as erase gates. In Embodiment 1 of the present invention, the upper surfaces of third gates 207a are positioned below the upper surfaces of floating gates 203b, whereby local increase in the electric field at the upper ends of the floating gates can be prevented during the erasing operation, and degradation of the interlayer dielectric film (insulator film 206a) can be suppressed after programming cycles, thereby assuring the reliability of memory cells.

In this structure, even if there are third gates 207a other than floating gates 203b and control

gates 211a, pitch in the wordline (WL) direction (direction x) and in the local data line direction (direction y) can be made twice as large as the minimum feature size. Thus, the memory cell area can be
5 reduced to minimum $4F^2$ (F: minimum feature size) in a cross-point type array.

Figs. 3 to 5 cross-sectionally show steps of a process for producing a semiconductor integrated circuit device according to Embodiment 1 of the present
10 invention.

At first, p-type (first conduction type) well 201 is formed in semiconductor substrate 200, and then gate insulator film (first insulator film) 202 is formed to a thickness at about 12 nm on well 201, for
15 example, by a thermal oxidation [Fig. 3(a)].

Then, phosphorus (P)-doped polysilicon film 203 to act as floating gates 203b and silicon nitride film 204 are successively deposited thereon [Fig. 3(b)]. Deposition of polysilicon film 203 and silicon
20 nitride film 204 can be carried out, for example, by CVD (chemical vapor deposition).

Then, said silicon nitride film 204 and polysilicon film 203 are patterned by lithography and dry etching. By the patterning, silicon nitride film
25 204 and polysilicon film 203 are made into silicon nitride films 204a and polysilicon films 203a, respectively [Fig. 3 (c)]. Silicon nitride films 204a and polysilicon films 203a are formed in a stripe form

by the patterning so that they are extended in the direction y.

Then, arsenic (As) ions are implanted into well 201 by tilted ion implantation to form diffusion layers 205 to act as sources/drains of memory cells [Fig. 3(d)]. Diffusion layers 205 function as source lines or data lines of memory cells. In the ion implantation, silicon nitride films 204a and polysilicon films 203a function as masks, so that diffusion layers 205 are formed as self-aligned to polysilicon films 203a. Since silicon nitride films 204a and polysilicon films 203a are formed in a stripe form as extended in the direction y, diffusion layers 205 are also formed as extended in the direction y. Since diffusion layers are formed by the tilted ion implantation, implanted ions are shielded by silicon nitride film 204a and polysilicon film 203a and thus diffusion layers 205 are not formed in the entire regions between adjacent polysilicon films 203a. Since the ions are implanted in the tilted direction, diffusion layers 205 are formed also partly under polysilicon films 203a, whereby parts each of third gates 207a and diffusion layers 205 are formed as overlapped with one another, as mentioned before, and thus channels are formed in well 201 under third gates 207a.

Since the members etched in the etching step (i.e. silicon nitride films 204a and polysilicon films

203a) contain neither metal films nor metal compound materials, no metals are dissolved in a cleaning step following the etching step and no dissolved metals redeposit on walls of the etched members. Thus, no
5 metals (impurities) are contained in silicon oxide film 206, which will be explained, referring to the next step, whereby defects of silicon oxide film 206 can be suppressed to minimum and the reliability can be improved.

10 Then, silicon oxide film 206 for isolating floating gates 203b from third gates 207a is formed in the following manner.

At first, the silicon oxide film is deposited to a thickness of about 10.5 nm by LPCVD (low pressure
15 chemical vapor deposition) [Fig. 3(e)]. Then, the silicon oxide film is annealed in an ammonia atmosphere to introduce nitrogen into said silicon oxide film 206. Then, nitrogen-introduced silicon oxide film 206 is subjected to wet oxidation to remove hydrogen
20 introduced into the silicon oxide film by annealing in ammonia.

Silicon oxide film 206 formed in the aforementioned manner has a small charge trapping and high programming/erasing endurance characteristics.
25 That is, if the charge is trapped in silicon oxide film 206, the trapped charges are transferred in a nonbiased state to third gates. The larger the amount of transferred electrons, the higher the possibility to

cause retention degradation. The amount of transferred electrons increase with trap density, and thus when the charge trapping is larger in silicon oxide film 206, probability to cause retention degradation will be increased. However in Embodiment 1 of the present invention, the charge trapping in the film is suppressed, the retention degradation will be suppressed and high programming/erasing endurance characteristics can be obtained. Furthermore, silicon oxide film 206 contains no metal impurities, as already mentioned above.

Then, phosphorus (P)-doped polysilicon film 207 to act as third gates 207a is deposited to completely fill gaps in floating gate pattern 203a [Fig. 4(a)]. The polysilicon film can be deposited, for example, by CVD.

Then, polysilicon film 207 is etched back, for example, by anisotropic dry etching, whereby third gates 207a were formed to a predetermined thickness as retained in the gaps in floating gate pattern 203a [Fig. 4(b)], where the thickness of retained polysilicon film (third gates 207a) following the etch back was made smaller than that of floating gate polysilicon 203a. Reliability of insulator film 206a for isolating floating gate polysilicon 203a from third gates 207a can be improved by forming third gates 207a of smaller thickness in this manner, whereby the retention degradation can be reduced as already

mentioned above.

Then, silicon oxide film 208 is deposited to completely fill the gaps in floating gate pattern 203a [Fig. 4(c)]. Deposition of silicon oxide film is
5 carried out, for example, by CVD.

Then, silicon oxide film 208 is polished, for example by CMP (chemical mechanical polishing) until silicon nitride films 204a are exposed (wherein silicon nitride films 204a and silicon oxide films 206 and 208
10 are made into silicon nitride films 204b, insulator films 206a and silicon oxide films 208a, respectively [Fig. 4(d)]).

Then, silicon nitride films 204b are removed with a hot aqueous phosphoric acid solution to expose
15 the surfaces of polysilicons 203a [Fig. 5(a)]. Then, phosphorus (P)-doped polysilicon film 209 is deposited [Fig. 5(b)] and subjected to anisotropic dry etching (whereby polysilicon film 209 are made into polysilicon films 209a) [Fig. 5(c)]. Polysilicon films 209a are
20 electrically connected to polysilicon 203a, and the polysilicons of those two layers form floating gates. polysilicons 209a are effective for increasing the surface area of floating gates, which results in and also increasing the coupling ratio of memory cells,
25 whereby the internal operating voltage can be reduced during the programming/erasing.

Nitrogen-introduced silicon oxide film (film thickness: about 10.5 nm) 210 for isolating floating

gates from word lines is formed in the same manner as shown in Figs. 3(e) [Fig. 5(d)].

Then, a stacked film of a polysilicon film, a tungsten nitride film and a tungsten film, i.e. so-called a polymetal film, is deposited and patterned by lithography and dry etching to form word lines 211a. The patterning is so carried out that word lines 211a are extended in the direction x, that is, in a vertical direction (direction x) to the direction of extended diffusion layers 205 and third gates 207a (direction y).

Furthermore, silicon oxide film 210 and polysilicon films 209a and 203a are etched to complete floating gates (whereby silicon oxide film 210 is made into 210a and polysilicons 203a and 209a are made into 203b and 209b, respectively) [Fig. 5(e)]. To etch silicon oxide film 210 in the etching step, etching is carried out under such conditions that only the silicon oxide film can be etched, whereas to etch polysilicon films 209a and 203a, etching is carried out under such selective etching conditions that silicon can be etched but no silicon oxide film is etched, where insulator films 208a as silicon oxide films function as an etching stopper, so that no third gates 207a under insulator films 208a are etched. That is, floating gates 203b are sectioned in both directions, i.e. direction x and direction y in the etching step to form island-form floating gates, while maintaining third

gates 207 in a stripe form as extended in the direction Y.

Then, an intermetal dielectric film is formed, and then contact holes are formed and connected with word lines 211a, source/drain diffusion layers 205, well 201 and third gates 207a, followed by deposition of a metal layer and patterning thereof to form wirings, thereby completing memory cells, though not shown in the drawing.

Fig. 6 is a graph showing relationships between programming/erasing cycles and threshold voltage when the memory cells formed in the aforementioned manner are subjected to programming/erasing cycles, and also showing together the data as to the memory cells formed by the art of Reference 1 as prior art for comparison.

In the prior art, the erasing speed is lowered when the programming/erasing cycles exceeds about 10^4 , and the threshold voltage is narrowed presumably for the following reasons.

That is, in the prior art, the upper surfaces of the floating gates would be in a lower position than the upper surfaces of the third gates. When an erase voltage is applied to the third gates in memory cells of such a structure, lines of electric force would be concentrated in convex parts at the upper surfaces of the floating gates, and the electric field of the interlayer dielectric film, which performs insulation

between polysilicon at the convex parts would be increased, as compared with the flat parts of side walls of floating gates. Thus, tunnel current would flow only through the convex parts at the upper
5 surfaces of the floating gates, and as a result the interlayer dielectric film at the parts in contact with the convex parts would be degraded in less programming/erasing cycles and electrons would be trapped. The electric field applied to the interlayer
10 dielectric film would be substantially reduced by such an electron trapping, so that the erasing speed would be lowered and the threshold voltage window would be narrowed.

In the memory cells according to Embodiment 1
15 of the present invention, on the other hand, the threshold voltage window is not substantially changed even after 10^6 programming/erasing cycles, because the convex parts on the upper surfaces of floating gates
209a are in contact with thick oxide films 208a, and
20 electron release takes place at the flat parts on side walls of floating gates 203b in case of erasing.

Fig. 7 is a graph showing results of measuring changes in the threshold voltage when to the memory cells according to Embodiment 1 of the present
25 invention are left standing after 10^6 programming/erasing cycles, and also shows results of prior art as measured in the same manner as already mentioned above.

In the prior art, it can be seen that the threshold voltage is largely lowered with increasing standing time, whereas in Embodiment 1 of the present invention no lowering of threshold voltage is observed, 5 because the interlayer dielectric film between the polysilicon is less degraded in case of the memory cells according to Embodiment 1 of the present invention than in the prior art, and leakage of electrons injected into the floating gates to the third 10 gates is suppressed.

Lower position of the upper surfaces of third gates than the position of the upper surfaces of floating gates is also effective for reduction of operating voltage.

15 Fig. 8 is a graph showing relationships between a difference in height between the upper surfaces of floating gates and the upper surfaces of third gates and a difference in voltage between the control gates and the third gates, when the erasing 20 operation is about to be completed after predetermined cycles, where the thickness of floating gates is made constant, and a difference in height is made positive when the upper surfaces of third gates are in a higher position than that of the upper surfaces of floating 25 gates, whereas a difference in height is made negative when the upper surfaces of third gates are in a lower position than that of the upper surfaces of floating gates. It can be seen from Fig. 8 that the voltage

between the third gates and the control gates can be lowered and the more the operating voltage can be reduced by the lower the position of the upper surfaces of third gates than that of the upper surfaces of floating gates.

When the upper surfaces of third gates are in a higher position than that of the upper surfaces of floating gates, short circuit takes place between the word lines and the third gates, resulting in occurrence of such a failure of conducting desired memory cell operation, and such a failure can be suppressed by bringing the upper surfaces of third gates into a lower position than that of the upper surfaces of floating gates.

Though the memory cells formed in the foregoing manner have third gates other than floating gates and control gates, the dimensions in the direction of local data lines and in the direction of word lines can be made twice as large as their respective minimum feature sizes F , and thus the memory cell area can be reduced to $4F^2$.

Embodiment 2

Fig. 9 cross-sectionally shows steps of a process for producing a semiconductor integrated circuit device according Embodiment 2 of the present invention. Differences of the process according to Embodiment 2 from that of Embodiment 1 are in lower

thickness of deposited polysilicon film to act as third gates than that of Embodiment 1, and coating of a photo resist onto the deposited polysilicon to fill the gaps in the floating gate pattern formed after the

5 polysilicon film deposition, followed by etching back the photo resist and the polysilicon to act as third gates at approximately equal speeds, thereby leaving only polysilicon in the gaps in the floating gate pattern. Arrangement of flash memory cells in plan

10 view, cross-sectional view of completed device and working system are the same as in Embodiment 1 and thus their explanation will be omitted below.

A process according to Embodiment 2 of the present invention will be described below. At first,

15 well 201, gate oxide film 203, floating gate patterns 203a and 204a, diffusion layers 205 and nitrogen-introduced silicon oxide film 206 for isolating floating gates from third gates are successively formed on silicon substrate 200 in the same manner as shown in

20 Fig. 3(a) - (e) of Embodiment 1 (not shown in drawing).

Then, phosphorus-doped polysilicon film 212 to act as third gates is deposited thereon so as not to fill the gaps in floating gate patterns 203a and 204a [Fig. 9(a)]. Thickness of polysilicon film 212 can be

25 made to correspond approximately to thickness of third gates after completion of memory cells.

Then, photo resist 213 is coated thereon to completely fill the gaps in floating gate patterns 203a

and 204a [Fig. 9(b)]. Then, said photo resist 213 and polysilicon film 212 are etched back at approximately equal speeds to leave only polysilicon film 212 to a predetermined thickness in the gaps in floating gate patterns 203a and 204a (whereby polysilicon 212 is made into 212a) [Fig. 9(c)]. Time required for the complete removal of the photo resist is defined as an etching end point.

Then, silicon oxide films 208a, floating gate polysilicon films 209a as a second layer, nitrogen-introduced silicon oxide film 210 and word lines 211a made from a polymetal film are formed thereon in the same manner as in Fig. 4(c) to Fig. 5(e) of Embodiment 1 to complete memory cells.

Memory cells formed in the foregoing manner can reduce fluctuation in thickness of third gaps 212a, as compared with Embodiment 1. That is, polysilicon film 212 is formed as a film and thickness of the film can be made to correspond to thickness of third gates, making it easier to control the film thickness. In Embodiment 2 of the present invention, photo resist 213 with good fluidity is coated, and thus the surface flatness of photo resist 213 at the time of etch-back starting can be improved, resulting in improved flatness of third gates after the etch-back.

Furthermore, in Embodiment 2 of the present invention, end point monitoring of etch-back can be more easily carried out by monitoring a plasma emission intensity

from photo resist 213, resulting in easier control of thickness of third gates. Furthermore, in Embodiment 2 of the present invention, use of photo resist 213 eliminates void formation in the gaps, resulting in improved etch-back controllability and easier thickness control of third gates. In Embodiment 1, on the other hand, the third gates are formed by etch-back in time control, and thus the thickness control is more difficult to conduct than in Embodiment 2 of the present invention. Thus, in Embodiment 2 fluctuation in coupling ratio between memory cells can be reduced and programming/erasing time can be made uniform.

As in Embodiment 1, narrowing of threshold voltage window can be suppressed during the programming/erasing in Embodiment 2, as compared with the prior art. Furthermore, changes in threshold voltage after standing can be suppressed, and operation can be carried out with a lower voltage. Occurrence of short circuit between the erase gates and floating gates can be also suppressed and memory cell area can be reduced to $4F^2$. Furthermore, program size and programming speed can be increased.

Embodiment 3

Fig. 10 cross-sectionally shows steps of a process for producing a semiconductor integrated circuit device according to Embodiment 3 of the present invention. A difference of the process according to

Embodiment 3 of the present invention from that of Embodiment 2 is in removal of polysilicon film on the floating gate patterns by CMP (chemical mechanical polishing) after deposition of the polysilicon film to
 5 act as third gates and before photo resist coating and etch-back. Arrangement of flash memory cells in plan view, cross-sectional structure of completed device and working system are the same as in Embodiment 1 and thus their explanation will be omitted below.

10 A process for producing the present memory cells is as follow. Well 201, gate oxide film 202, floating gate patterns 203a and 204a, diffusion layer 205 and nitrogen-introduced silicon oxide film 206 for isolating floating gates from third gates are
 15 successively formed on silicon substrate 200 in the same manner as shown in Fig. 3(a) - (e) of Embodiment 1 (not shown in drawing).

Then, phosphorus-doped polysilicon film 214 to act as third gates is deposited thereon so as not to
 20 fill the gaps in floating gate patterns 203a and 204a [Fig. 10(a)]. Thickness of polysilicon film 214 is made to correspond approximately to thickness of third gates of completed memory cells.

Then, said polysilicon film 214 is removed by
 25 polishing, i.e. by CMP until silicon nitride films 204a of floating gate pattern are exposed (whereby polysilicon film 214 and silicon oxide film 206 are made into 214a and 206a, respectively) [Fig. 10(b)].

Then, photo resist 215 is coated thereon to completely fill the gaps in floating gate patterns 203a and 204a [Fig. 10(c)]. Then, said photo resist 215 and polysilicon films 214a are etched back at approximately
5 equal speeds to leave only polysilicon films 214a to a predetermined thickness in the gaps of floating gate patterns 203 and 204a (whereby polysilicon films 214a are made into 214b) [Fig. 10(a)]. Time required for complete removal of the photo resist is defined as an
10 etching end point.

Then, silicon oxide films 208a, floating gate polysilicon films 209 as a second layer, nitrogen-introduced silicon oxide film 210 and word lines 211a made from a polymetal film are formed thereon in the
15 same manner as shown in Fig. 4(c) - Fig. 5(e) of Embodiment 1 to complete memory cells.

The memory cells formed in the foregoing manner can much more reduce fluctuation in thickness of third gates 214b than in Embodiment 2. That is, in
20 Embodiment 3, the upper surface of polysilicon film 214 is polished by CMP in advance, and thus an etching amount of polysilicon can be reduced, and as a result thickness of third gates 214b can be made smaller. That is, fluctuation in coupling ratio between the
25 memory cells can be made lower, and programming/erasing time can be made uniform.

As in Embodiment 1, narrowing of threshold voltage window can be suppressed during the programming

in Embodiment 3, as compared with the prior art. Furthermore, changes in threshold voltage after standing can be suppressed and operation can be carried out with a lower voltage. Occurrence of short circuit
5 between the erase gates and the floating gates can be also suppressed and memory cell area can be reduced to $4F^2$. Furthermore, program size and programming speed can be increased.

As shown in Fig. 11, silicon oxide film 214' (e.g. a TEOS oxide film, an SOG film, etc.) can be formed before polishing polysilicon film 214 by CMP [Fig. 11(a)], and said silicon oxide film 214' and polysilicon film 214 can be polished together by CMP (whereby silicon oxide film 214' is made into 214a')
10 [Fig. 11(b)]. In that case, polysilicon film 214 never falls down inwardly into the gaps and is never damaged. Then, silicon oxide films 214a' are selectively removed, followed by steps of Fig. 10(b) et seq.

Embodiment 4

20 Figs. 12 and 13 cross-sectionally show steps of a process for producing a semiconductor integrated circuit device according to Embodiment 4 of the present invention. A difference of the process of Embodiment 4 from that of Embodiment 2 is in formation of a silicon
25 oxide film after deposition of a polysilicon film to act as third gates and its use as a protection film for etch-back. Arrangement of flash memory cells in plan

view, cross-sectional structure of completed device and working system are the same as in Embodiment 1 and thus their explanation will be omitted below.

At first, well 201, gate oxide film 202,
 5 floating gate patterns 203a and 204a, diffusion layers 205 and nitrogen-introduced silicon oxide film 206 for isolating floating gates from third gates are successively formed on silicon substrate 200 in the same manner as shown in Fig. 3(a) - (e) of Embodiment 1
 10 (not shown in drawing).

Then, phosphorus-doped polysilicon film 216 to act as third gates is deposited thereon so as not to completely fill the gaps in floating gate patterns 203a and 204a [Fig. 12(a)]. Thickness of polysilicon film
 15 216 is made approximately to correspond to the thickness of third gates of completed memory cells.

Then, silicon oxide film 217 to act as a protection film when polysilicon film 216 is to be etched back is formed thereon [Fig. 12(b)].

20 Then, said polysilicon film 216 and silicon oxide film 217 are removed by polishing, i.e. CMP, until silicon nitride films 204a of floating gate pattern are exposed (whereby polysilicon film 216, and silicon oxide films 206 and 217 are made into 216a,
 25 206a and 217a, respectively) [Fig. 12(c)].

Then, polysilicon films 216a is etched back to leave polysilicon films 216a to a predetermined thickness in the gaps in floating gate patterns 203a

and 204a (whereby polysilicon 216a are made into 216b) [Fig. 13(a)].

Then, silicon oxide films 217a retained in the gaps in floating gate patterns 203a and 204a are removed by wet etching [Fig. 13(b)].

Then, silicon oxide films 208a, floating gate polysilicon films 209a as a second layer, nitrogen-introduced silicon oxide film 210 and word lines 211a made from a polymetal film are formed in the same manner as shown in Fig. 4(c) - Fig. 5(e) of Embodiment 1 to complete memory cells.

As in Embodiments 1 to 3, memory cells formed in Embodiment 4 can suppress narrowing of threshold voltage window during the programming, as compared with the prior art. Furthermore, changes in threshold voltage after standing can be suppressed and operation can be carried out with a lower voltage. Occurrence of short circuit between the erase gates and the floating gates can be also suppressed and memory cell area can be reduced to $4F^2$. Furthermore, program size and programming speed can be increased.

In Embodiment 4, since silicon oxide films 217a are formed in the central regions where third gates 216b are in a finished state, side wall regions of silicon oxide films 217a, as not covered silicon oxide films 217a (both end regions of third gates 216b) are selectively etched. Thus, cross-section of both etched end regions can be made into a sufficiently flat

shape even in the side wall regions in the finished state of third gates 216b [Fig. 13(c)]. That is, the etching speed of the side wall regions is lower in the ordinary etching, and thus the side wall regions are
5 etched into a shape with sharp projection P in the side wall regions [Fig. 13(d)].

In Embodiment 4, silicon oxide films 217a to act as a mask are formed in the central regions, as already mentioned before, no such shape is formed.
10 Thus, the height of third gates 216b can be surely made lower than that of floating gates 203a, and the object of the present invention can be attained successfully.

As shown in Fig. 14, thick silicon oxide films 217c may be formed to fill the gaps in place of
15 silicon oxide film 217 [Fig. 14(a)]. Then, silicon oxide film 217c and polysilicon film 216 are polished by CMP [Fig. 14(b)], whereby silicon oxide film 217c is made into silicon oxide films 217d, and polysilicon film 216 is made into polysilicon films 216a). Then,
20 polysilicon films 216a are etched back in the same manner as mentioned above, to leave polysilicon films 216a to a predetermined thickness in the gaps in floating gate patterns 203a and 204a (whereby polysilicon films 217d are made into 216b) [Fig.
25 14(c)]. Then, silicon oxide films 217d are removed, followed by steps of Fig. 13(b) et seq. In that case, falling-down of polysilicon film 216 inwardly into the gaps by CMP and the resulting damages can be prevented.

Embodiment 5

Fig. 15 cross-sectionally shows steps of a process for producing a semiconductor integrated circuit device according to Embodiment 5 of the present invention. In Embodiment 5, chemical mechanical polishing and etching-back by dry etching are used together to process the polysilicon film to act as third gates. Arrangement of flash memory cells in plan view, cross-sectional structure of completed device and working system are the same in Embodiment 1 and thus their explanation will be omitted below.

At first, well 201, gate oxide film 202, floating gate patterns 203a and 204a, diffusion layers 205 and nitrogen-introduced silicon oxide film 206 for isolating floating gates for third gates are successively formed on silicon substrate 200 in the same manner as shown in Fig. 3(a) - (e) of Embodiment 1 (not shown in drawing).

Then, phosphorus-doped polysilicon film 218 to act as third gates is deposited thereon to completely fill the gaps in floating gate patterns 203a and 204a [Fig. 15(a)].

Then, said polysilicon film 218 is removed by polishing, i.e. CMP, until silicon nitride film 204a of floating gate pattern are exposed (whereby polysilicon film 218 and silicon oxide film 206 are made into 218a and 206a, respectively) [Fig. 15(b)].

Then, polysilicon films 218a are etched back

to leave polysilicon films 218a to a predetermined thickness in the gaps in floating gate patterns 203a and 204a (whereby polysilicons 218a are made into 218b) [Fig. 15(c)].

5 Then, silicon oxide films 208a, floating gate polysilicon films 209a as a second layer, nitrogen-introduced silicon oxide film 210 and word lines 211a made from a polymetal film are successively formed thereon in the same manner as in Figs. 4(c) to Fig. 10 5(e) of Embodiment 1 to complete memory cells.

As in Embodiments 1 to 4, memory cells formed in Embodiment 5 can suppress narrowing of threshold voltage window during the programming, as compared with the prior art. Furthermore, changes in threshold 15 voltage after standing can be suppressed and operation can be carried out with a lower voltage. Occurrence of short circuit between the third gates and the floating gates can be also suppressed and memory cell area can be reduced to $4F^2$. Furthermore program size and 20 programming speed can be increased.

In the process of Embodiment 5, polysilicon film 218 is polished as shown in Fig. 15(b), and thus the surface is flattened. An amount of polysilicon to be removed by successive etching-back can be reduced 25 and thus load in the etching-back step can be reduced. Furthermore, etching is carried out after the flattening, and thus the surface of polysilicon films 218b can be easily made flat.

Embodiment 6

Figs. 16 and 17 cross-sectionally show steps of a process for producing a semiconductor integrated circuit device according to Embodiment 6 of the present invention. Difference of Embodiment 6 from Embodiments 1-5 is in adjustment of the height of the upper surface of polysilicon film to act as third gates by thermal oxidation. Arrangement of flash memory cells in plan view, cross-sectional structure of completed device and working system are the same as in Embodiment 1 and thus their explanation will be omitted below.

At first, well 201, gate oxide film 202, floating gate patterns 203a and 204a, diffusion layers 205 and nitrogen-introduced silicon oxide film 206 for isolating floating gates from third gates are successively formed on silicon substrate 200 in the same manner as shown in Fig. 3(a) - (e) of Embodiment 1 (not shown in drawing).

Then, phosphorus-doped polysilicon film 219 to act as third gates are deposited thereon to completely fill the gaps in floating gate patterns 203a and 204a [Fig. 16(a)].

Then, polysilicon film 219 is etched back by anisotropic dry etching to leave the film in the gap in floating gate patterns 203a (whereby polysilicon 219 is made into 219a) [Fig. 16(b)].

Then, silicon oxide film 220 is formed on the surfaces of polysilicon films 219a by thermal oxidation

to bring the upper surfaces of polysilicons 219a into a desired position lower than floating gate polysilicon 203a (whereby polysilicon 219a are made into 219b) [Fig. 16(c)], where nitrogen in silicon oxide film 206 is advantageously effective for suppressing oxidation of side walls of floating gate polysilicon 203a.

Then, silicon oxide film 206 present on the upper surfaces of silicon nitride film patterns 204a is removed by an aqueous hydrofluoric acid solution (whereby silicon oxide film is made into 206b) [Fig. 17(a)].

Then, silicon nitride films 204 are removed by a hot aqueous phosphoric acid solution to expose the surfaces of polysilicons 203a [Fig. 17(b)].

The successive steps are the same as those of Fig. 5(b) et seq. of Embodiment 1.

In Embodiment 6, fluctuation in thickness of third gates 219b can be reduced, as compared with Embodiments 1 to 5. That is, in the etch-back step of Fig. 16(b), the surfaces of polysilicon films 219a formed in the gaps between the floating gates can be obtained in a relatively shallow position, and thus can be made flat. Furthermore, silicon oxide film 220 is formed by thermal oxidation, and thus its thickness control can be made more easily. Thus, third gates 219b can be formed under good controllability, so that function in the thickness can be controlled. As a result, fluctuation in coupling ratio between the

memory cells can be reduced and programming/erasing time can be made uniform.

As in Embodiment 1, narrowing of threshold voltage window can be suppressed during the programming
5 in Embodiment 6, as compared with the prior art. Furthermore, changes in threshold voltage after standing can be suppressed and operation can be carried out with a lower voltage. Occurrence of short circuit between the erase gates and the floating gates can be
10 also suppressed and memory cell area can be reduced to $4F^2$. Furthermore, program size and programming speed can be increased.

Embodiment 7

Figs. 18-20 cross-sectionally show steps of a
15 process for producing a semiconductor integrated circuit device according to Embodiment 7 of the present invention. Different from Embodiments 1 to 6, Embodiment 7 shows a case of forming third gates before formation of floating gate patterns. Arrangement of
20 flash memory cells in plan view, and working system are the same as in Embodiment 1 and thus their explanation will be omitted below.

At first, p-type well 301 is formed in silicon substrate 300 and then gate oxide film 302 is
25 formed thereon to a thickness of about 12 nm, for example, by thermal oxidation [Fig. 18(a)].

Then, phosphorus-doped polysilicon film 303

and silicon oxide film to act as third gates are successively deposited thereon [Fig. 18(b)].

Then, said silicon oxide film 304 and polysilicon film 303 are patterned by lithography and
5 dry etching (whereby silicon oxide film and polysilicon film are made into 304a and 303a, respectively) [Fig. 18(c)].

Then, arsenic ions are implanted by tilted ion implantation to form diffusion layers 305 to act as
10 source/drains of memory cells [Fig. 18(d)].

Then, nitrogen-introduced silicon oxide film 306 for isolating floating gates from third gates is formed in the same manner as in Fig. 3(e) of Embodiment 1 [Fig. 19(a)], and phosphorus-doped polysilicon film
15 307 to act as floating gates is deposited to completely fill the gaps in third gate patterns 303a and 304a [Fig. 19(b)].

Then, polysilicon film 307 is etched back by anisotropic dry etching to leave it in the gaps in
20 third gate patterns 303a and 304a (whereby polysilicon 307 is made into 307a), where an etching amount is so adjusted that the surfaces of polysilicon films 307a are in a higher position than that of the surfaces of polysilicon films 303a [Fig. 19(c)].

25 Then, phosphorus-doped polysilicon film 308 is deposited thereon [Fig. 19(d)] and then subjected to anisotropic dry etching (whereby polysilicon film 308 is made into 308a) [Fig. 20(a)]. Said polysilicon

films 308a are electrically connected to polysilicons 307a, and two layers of these polysilicons form floating gates. Polysilicons 308a are effective for increasing the floating gate surface area and also
5 increasing coupling ratio of memory cells, whereby internal operating voltage during programming/erasing can be reduced.

Then, nitrogen-introduced silicon oxide film 309 for isolating floating gates from word lines is
10 formed thereon to a thickness of 10.5 nm in the same manner as shown in Fig. 3(e) [Fig. 20(b)].

Then, so called polymetal film 310, i.e. a stacked film of a polysilicon film, a tungsten nitride film and a tungsten film, is deposited thereon and
15 patterned by well known lithography and dry etching to form word lines (whereby polymetal film 310 is made into 310a). Furthermore, silicon oxide film 309, and polysilicon films 308a and 307a are successively etched to complete floating gates (whereby polysilicons 308a
20 and 307a are made into 308b and 307b, respectively, and silicon oxide film 309 into 309a) [Fig. 20(c)].

Then, after formation of an intermetal dielectric film, contact holes in communication with word lines 310a, source/drain diffusion layers 305,
25 well 301 and third gates 303a are formed and then a metal film is deposited thereon and patterned to form wirings, thereby completing memory cells, though not shown in drawing.

In memory cells formed according to Embodiment 7, fluctuation in programming/erasing time between bits can be reduced, as compared with Embodiments 1 to 6, because in Embodiment 7 the position of upper surfaces of third gates depends on deposited film thickness of polysilicon film, and thus fluctuation in coupling ratio between the memory cells can be reduced.

Furthermore, filling of the gaps between floating gate patterns 203a by silicon oxide film 208 and flattening by CMP of Embodiments 1 to 5 are not required in Embodiment 7, simplifying process steps.

As in other Embodiments, narrowing of threshold voltage window can be suppressed during the programming in Embodiment 7, as compared with the prior art. Furthermore, changes in threshold voltage after standing can be suppressed and operation can be carried out with a lower voltage. Occurrence of short circuit between the third gates and the floating gates can be also suppressed and memory cell area can be reduced to $4F^2$. Furthermore, program size and programming speed can be increased.

Embodiment 8

Fig. 21 cross-sectionally shows steps of a process for producing a semiconductor integrated circuit device according to Embodiment 8 of the present invention. The process of Embodiment 8 shows another

case of forming third gates before forming a floating gate pattern. Arrangement of flash memory cells in plan view and working system are the same as in Embodiment 1, and thus their explanation will be
5 omitted below.

p-Type well 301, gate oxide film 302, polysilicon films 303a and silicon oxide films 304a are successively formed on silicon substrate 300, and diffusion layers 305 to act as sources/drains of memory
10 cells and nitrogen-introduced silicon oxide film 306 are formed in the same manner as shown in Fig. 18(a) to Fig. 19(a) of Embodiment 7 (not shown in drawing).

Then, phosphorus-doped polysilicon film 311 to act as floating gates is deposited thereon, where,
15 different from Embodiment 7, thickness of polysilicon film 311 is selected so as not to completely fill the gaps in third gate patterns 303a and 304a [Fig. 21(a)].

Then, polysilicon film 311 is removed by polishing, e.g. CMP, until the upper surfaces of
20 silicon oxide films 304a are exposed (whereby polysilicon film 311 are made into 311a, and silicon oxide films 304a and 306 are made into 304b and 306a, respectively) [Fig. 21(b)]. Here, the polishing is exemplified by CMP, but etching-back may be used, or
25 etching-back may be carried out after filling the gaps with a photo resist, or CMP may be carried out by filling the gaps with a silicon oxide film.

Then, nitrogen-introduced silicon oxide film

310 for isolating floating gates from word lines is formed to a thickness of about 10.5 nm in the same manner as shown in Fig. 3(e) [Fig. 21(c)].

Then, so-called polymetal film 310, i.e. a
5 saked film of a polysilicon film, a tungsten nitride film, and a tungsten film, is deposited thereon, and patterned by well known lithography and dry etching to form word lines (whereby polymetal film 310 is made into 310a). Furthermore, silicon oxide film 309 is
10 etched to complete floating gates (whereby silicon oxide 309 into 309a) [Fig. 21(d)].

Then, after forming an intermetal dielectric film, contact holes in connection with word lines 310a, source/drain diffusion layers 305, well 301 and third
15 gates 303a are formed, and then a metal film is formed and patterned to form wirings, thereby completing memory cells (not shown in drawing).

In memory cells formed according to Embodiment 8, fluctuation in programming/erasing time
20 between bits can be reduced. Since the floating gates are formed from a single layer of polysilicon, the process steps can be more simplified than those of Embodiment 7.

Furthermore, as in other Embodiments,
25 narrowing of threshold voltage window can be suppressed during the programming in Embodiment 8, as compared with the prior art. Furthermore, changes in threshold voltage after standing can be suppressed and operation

can be carried out with a lower voltage. Occurrence of short circuit between the third gates and the floating gates can be also suppressed and memory cell area can be reduced to $4F^2$. Furthermore, program size and
5 programming speed can be increased.

Embodiment 9

Figs. 22-24 cross-sectionally show steps of a process for producing a semiconductor integrated circuit device according to Embodiment 9 of the present
10 invention.

At first, p-type well 401 is formed in silicon substrate 400, and field oxide film 402 to act as an isolation region is formed thereon [Fig. 22(a)]. Then, gate oxide film 403 is formed by thermal
15 oxidation [Fig. 22(b)].

Then, phosphorus-doped polysilicon film 404 to act as floating gates are deposited thereon [Fig. 22(c)], and patterned by lithography and dry etching to form floating gates (whereby polysilicon film is made
20 into 404a) [Fig. 22(d)].

Then, arsenic ions are implanted therein by ion implantation to form diffusion layers 405 to act as sources/drains of memory cells (not shown in drawing).

Then, insulator film 405 for isolating
25 floating gates from third gates is formed in the same manner as shown in Fig. 3(e) of Embodiment 1 [Fig. 23(a)].

Then, phosphorus-doped polysilicon film 410 to act as third gates are deposited thereon to completely fill the gaps in floating gate patterns 404a [Fig. 23(b)].

5 Then, polysilicon film 410 is etched back by dry etching so that the upper surface of polysilicon film 410 can be in a lower position than that of upper surfaces of floating gate polysilicons 404a (whereby polysilicon 410 is made into 410a) [Fig. 23(c)].

10 Then, nitrogen-introduced silicon oxide film 408 for isolating floating gates from word lines is formed in the same manner as shown in Fig. 3(e) of Embodiment 1 [Fig. 24(a)].

20 Then, so called polymetal film 409, i.e. a stacked film of a polysilicon film, a tungsten nitride film and a tungsten film, is deposited thereon [Fig. 24(b)], and then patterned by lithography and dry etching to form word lines (whereby polymetal film 409 is made into 409a) [Fig. 24(c)].

25 Then, after forming an intermetal dielectric film, contact holes in communication with word lines 409a, source/drain diffusion layers 405, well 401 and third gates 407a are formed, and then a metal layer is deposited and patterned to form wirings, thereby completing memory cells (not shown in drawing).

In memory cells formed according to Embodiment 9, narrowing of threshold voltage window can be suppressed during programming/erasing cycles, as

compared with the prior art. Furthermore, changes in threshold voltage after standing can be suppressed and operation can be carried out with a lower voltage.

According to Embodiment 9, reliability of a semiconductor integrated circuit device after programming/erasing cycles can be effectively improved and internal operating voltage can be effectively reduced.

In the foregoing, the present invention has been described in detail, referring to Embodiments, but the present invention shall not be limited only to the foregoing Embodiments, but, needless to say, can be variously modified within the spirit and the scope of the present invention.

For example, in the foregoing embodiments, a stacked film of a polysilicon film, a tungsten nitride film and a tungsten film is used as materials for word lines, but even other barrier metal films, e.g. films of a transition metal element itself, such as tungsten, titanium, tantalum, etc., or its nitrides, or its silicides, or an aluminum nitride, a cobalt silicide film, a molybdenum silicide film or alloy films such as a titanium-tungsten film, etc. can be used to obtain equivalent effects in place of the tungsten nitride film. Furthermore, even a stacked film of a polysilicon film and a metal silicide film, i.e. so-called polycide film, can have an equivalent effect. Typical example of the metal silicide film is a

tungsten silicide film. Even a polysilicon monolayer film has an equivalent effect.

In the foregoing Embodiments, a nitrogen-introduced silicon oxide film is used as an insulator film for isolating floating gates from third gates, but when the present non-volatile semiconductor memory device is applied to products of less programming/erasing cycles, a silicon oxide film formed by conventional thermal oxidation or CVD may be used.

In the foregoing Embodiments, a nitrogen-introduced silicon oxide film is also used as an insulator film for isolating floating gates from control gates, but when the device is applied to cases where the internal operating voltage during the programming/ erasing or programming/erasing speed is not so important, a so far widely used stack film of silicon oxide film/silicon nitride film/silicon oxide film, i.e. a so-called ONO film may be used as the insulator film.

In the foregoing Embodiments, description has been made of n-channel type memory cells, in which n-type diffusion layers are formed in p-type well, but p-channel type memory cells, in which the diffusion layers are of p-type, have an equivalent effect. In that case, voltages of control gates, third gates and drains during the programming/erasing will be negative, relative to the well voltage. In that case, electron injection is made by hot electrons.

In the foregoing Embodiments, the third gates have both functions of gates for controlling split channels and of erase gates during the programming/erasing, but may have any one of the functions.

5 Industrial Applicability

In the foregoing Embodiments, necessary levels of electrons injected into floating gates during programming/erasing are minimum two, but the present invention may be applied to so-called multilevel storage of forming at least 4 levels and storing at least 2 bits in one memory cell. In the conventional multilevel storage, there has been a problem of a larger difference between the lowest threshold voltage level and the highest threshold voltage level, as compared with two-level storage, even if the amount of electrons injected into the floating gates is precisely controlled to compress the threshold voltage distribution on the respective levels. Thus, in the Fowler-Nordheim type programming/erasing, there has been such a problem that the programming/erasing speed is retarded or the programming/erasing voltage is increased. In the present invention, programming and erasing can be carried out with a lower voltage such as 13.5 V or lower. In other words, the programming/erasing can be carried out at a higher speed, and thus the present invention is very effective for the multilevel storage system.

Furthermore, the present invention can be widely applied to semiconductor devices provided with a memory cell array having an non-volatile semiconductor memory device, e.g. one-chip microcomputers, system

5 LSI, etc.

Typical effects of the present invention can be summarized as follows: improved reliability of a semiconductor integrated circuit device after programming/erasing cycles; reduced internal operating

10 voltage of a semiconductor integrated circuit device; improved yield of a semiconductor integrated circuit device; reduced memory cell area of a semiconductor integrated circuit device; and improved operating speed of a semiconductor integrated circuit device.

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FIG. 2

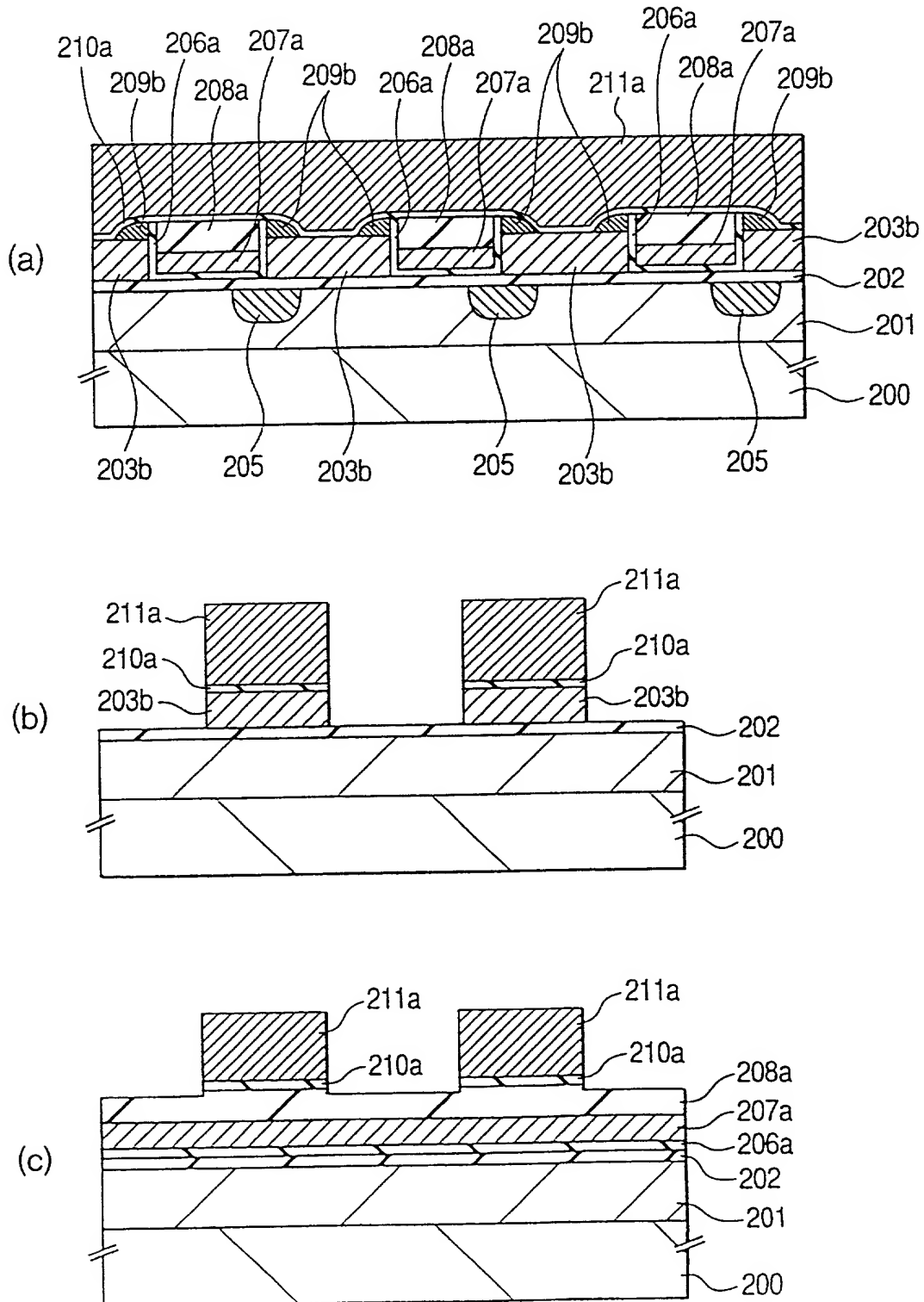


FIG. 3

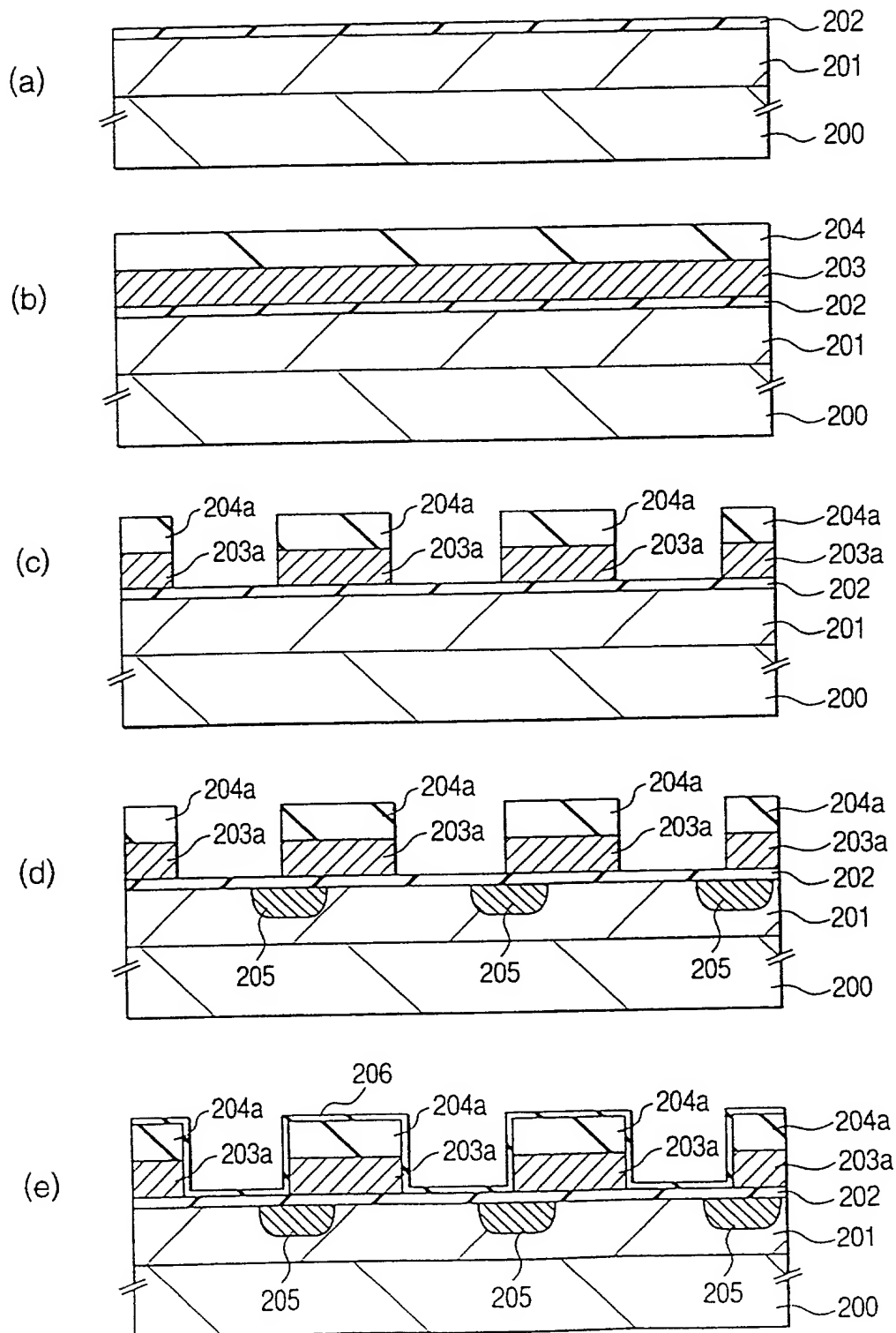
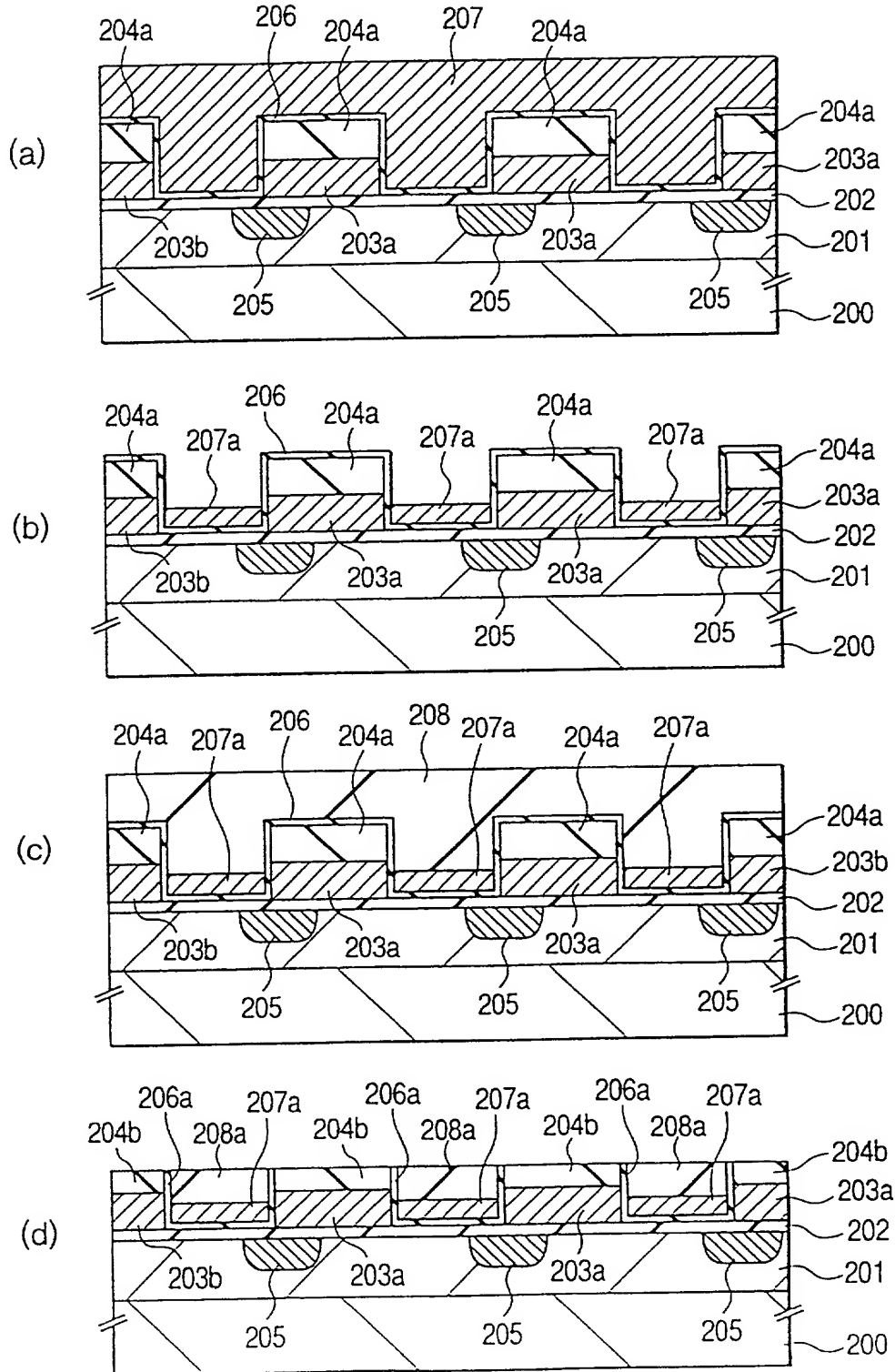


FIG. 4



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FIG. 5

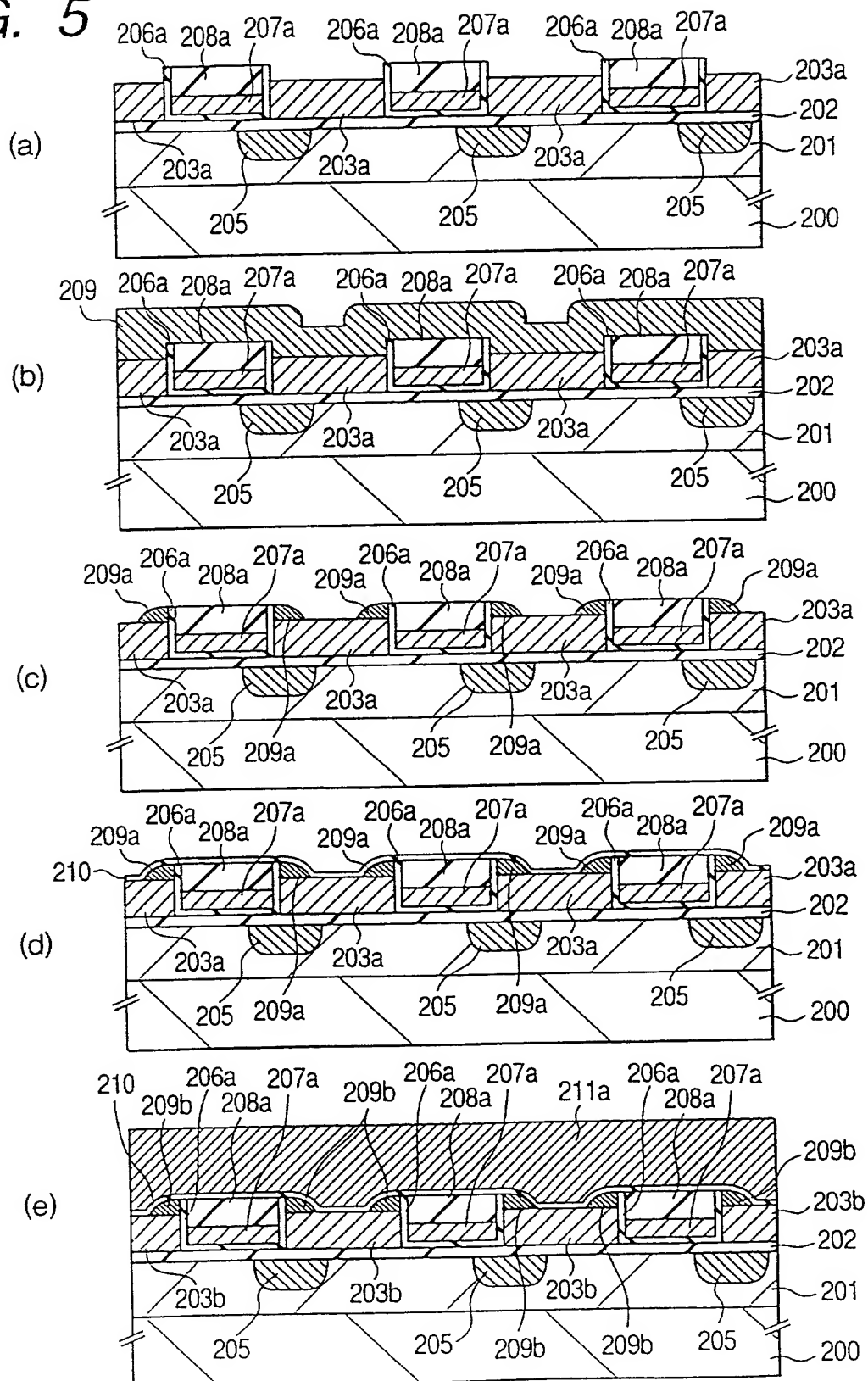


FIG. 6

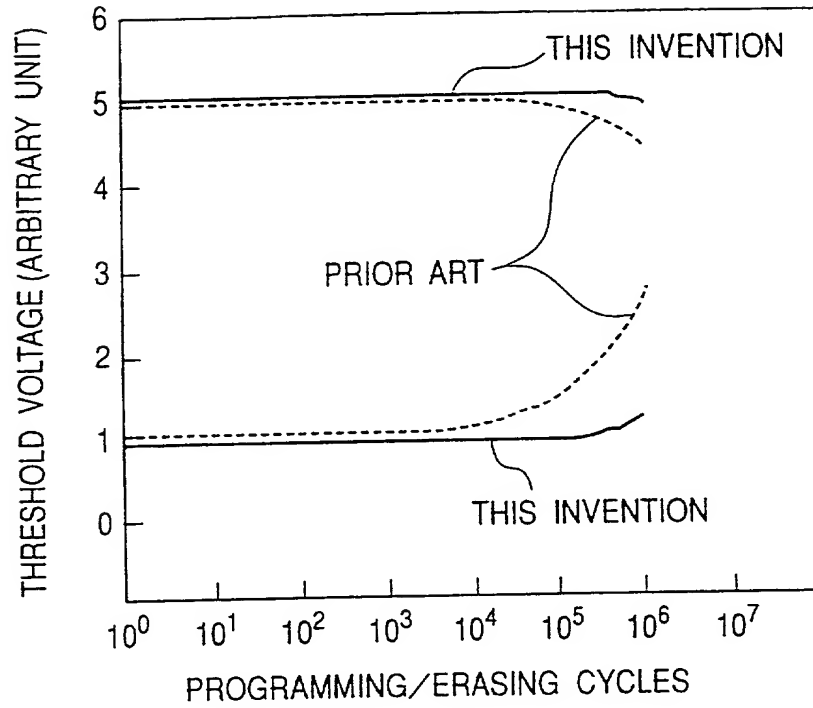
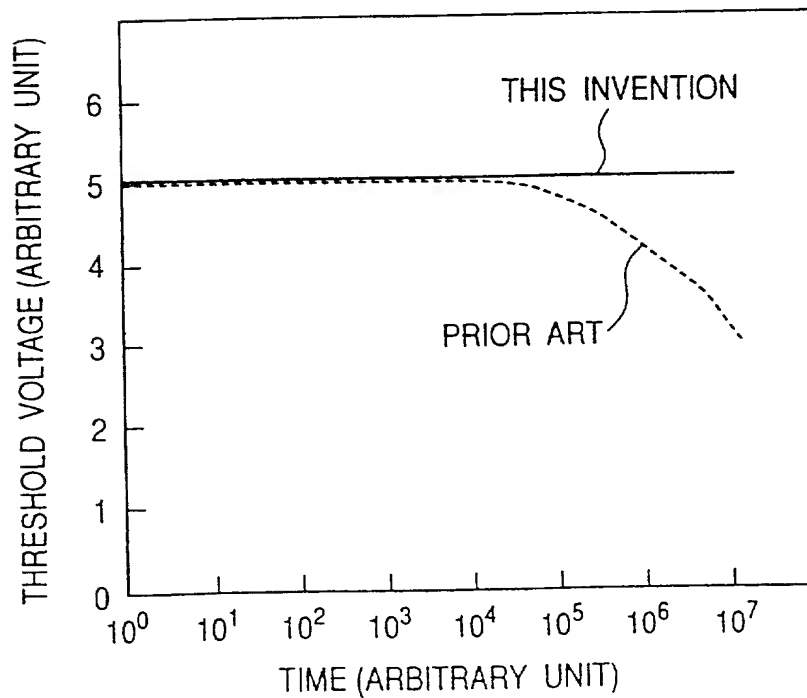
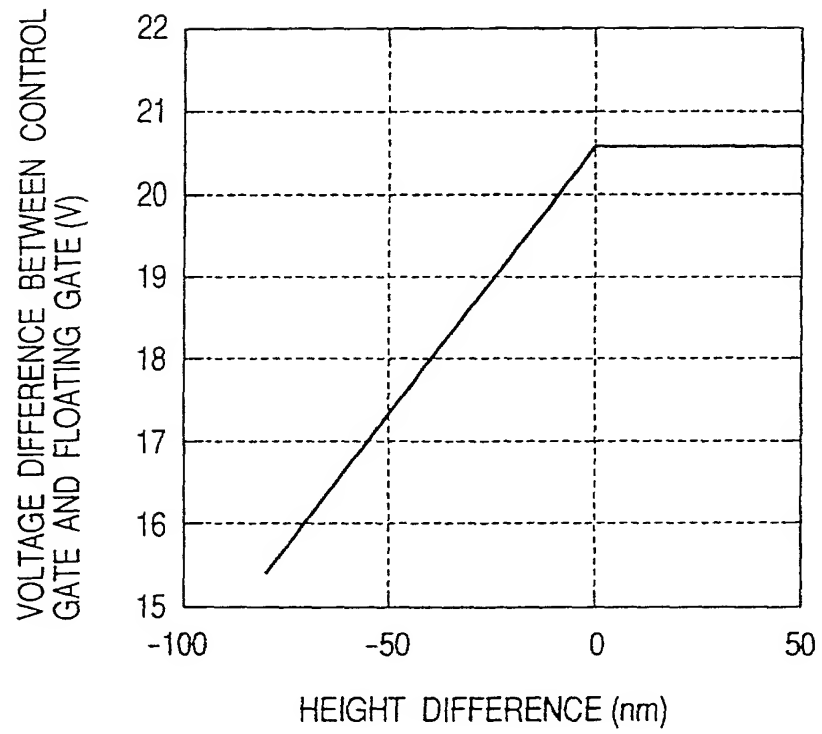


FIG. 7



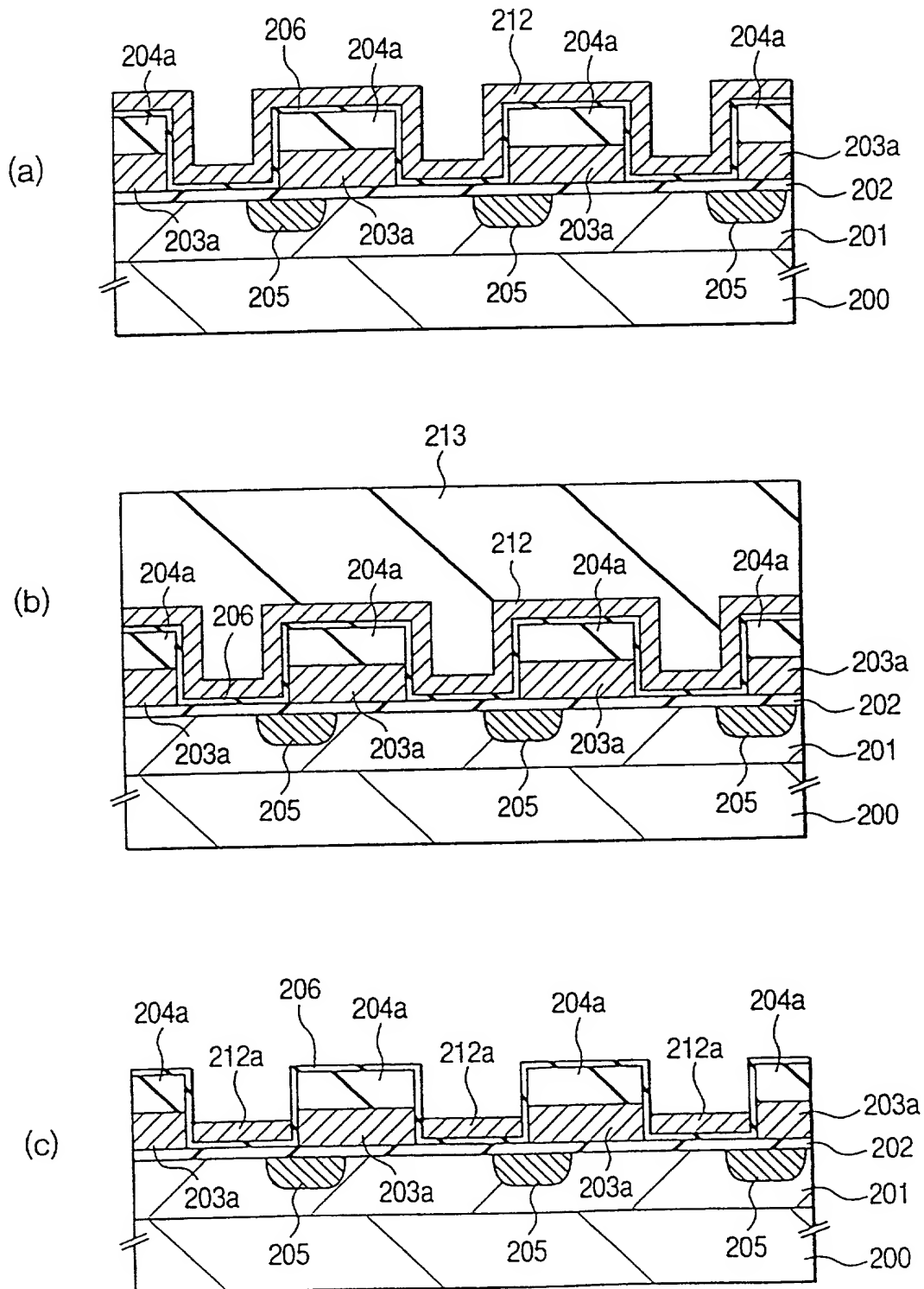
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FIG. 8



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FIG. 9



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FIG. 10

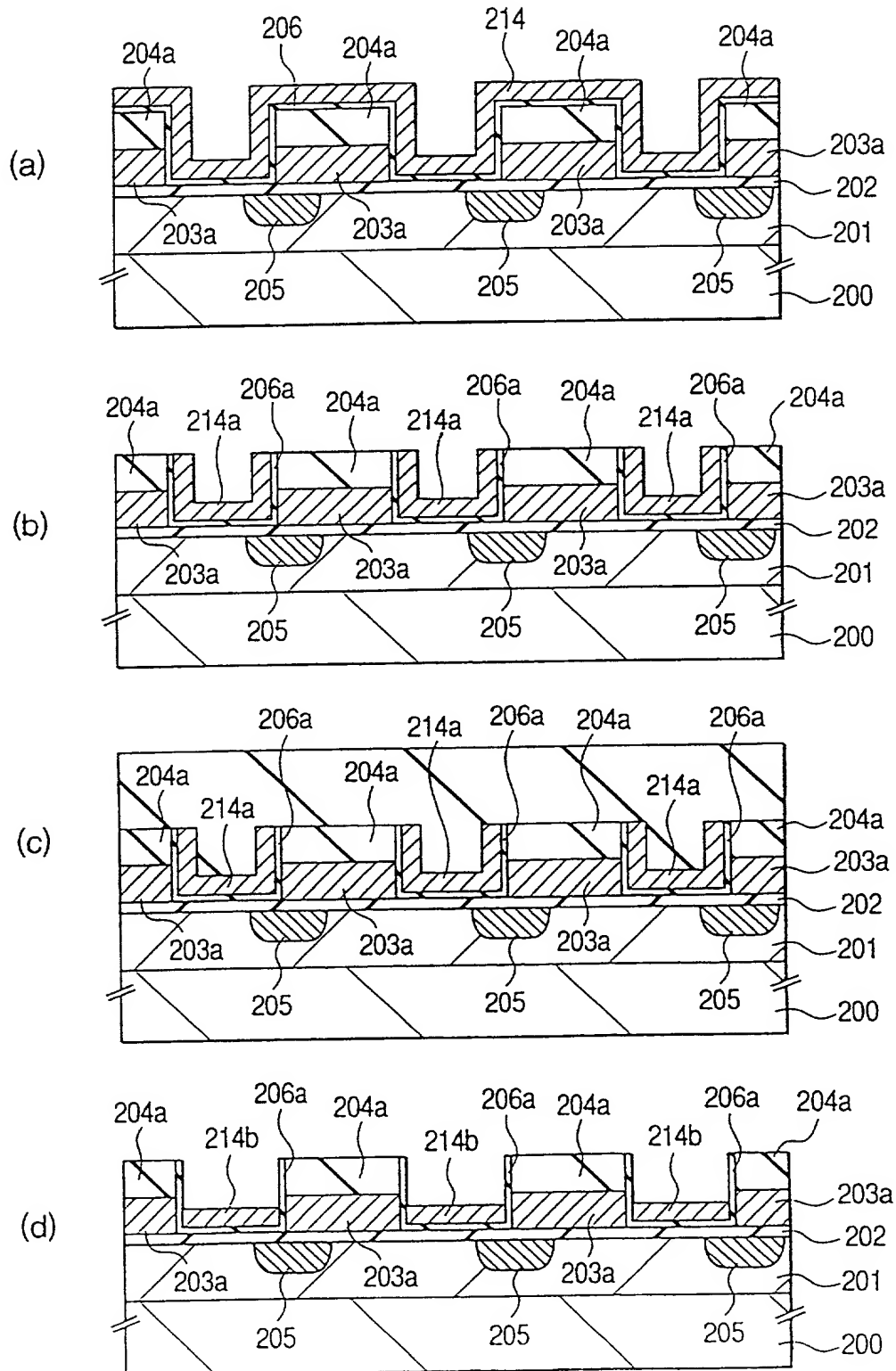
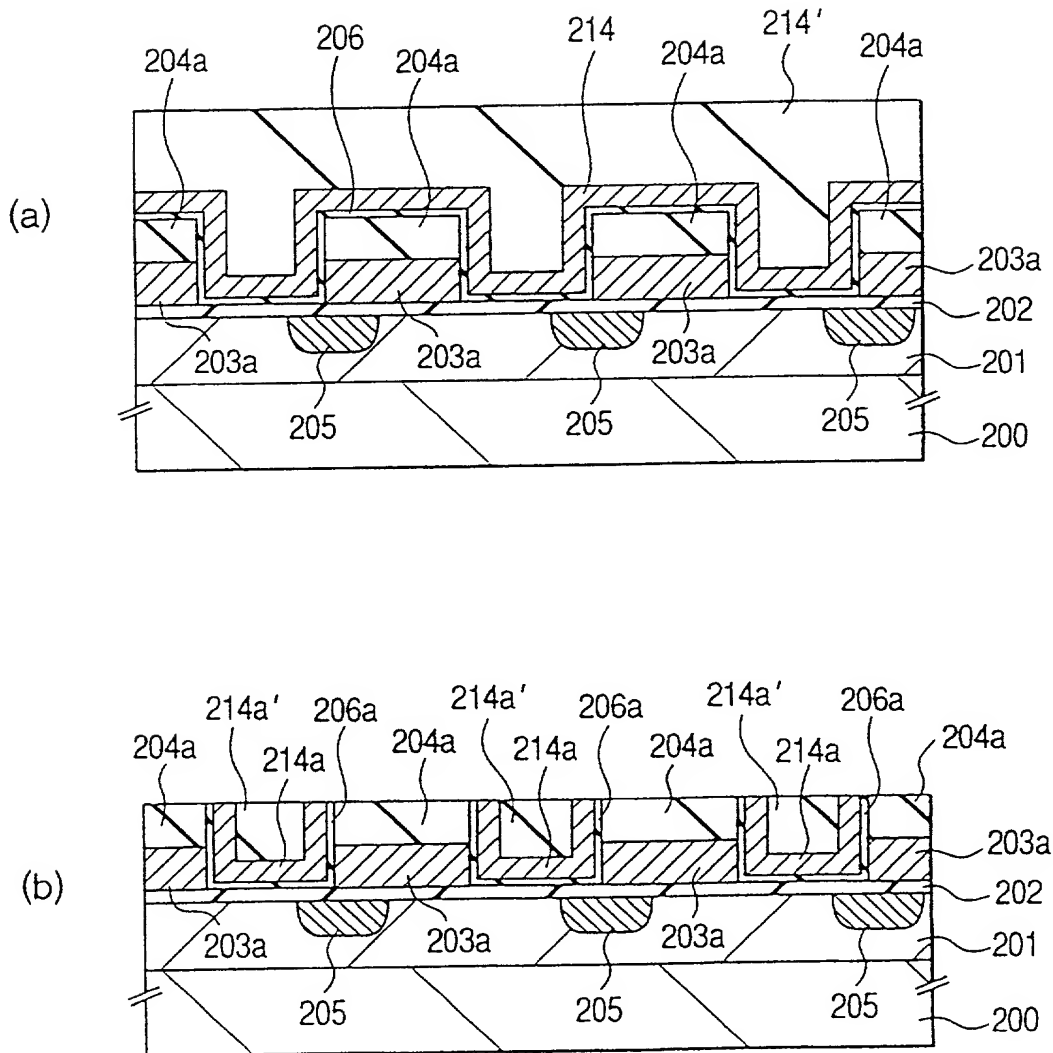
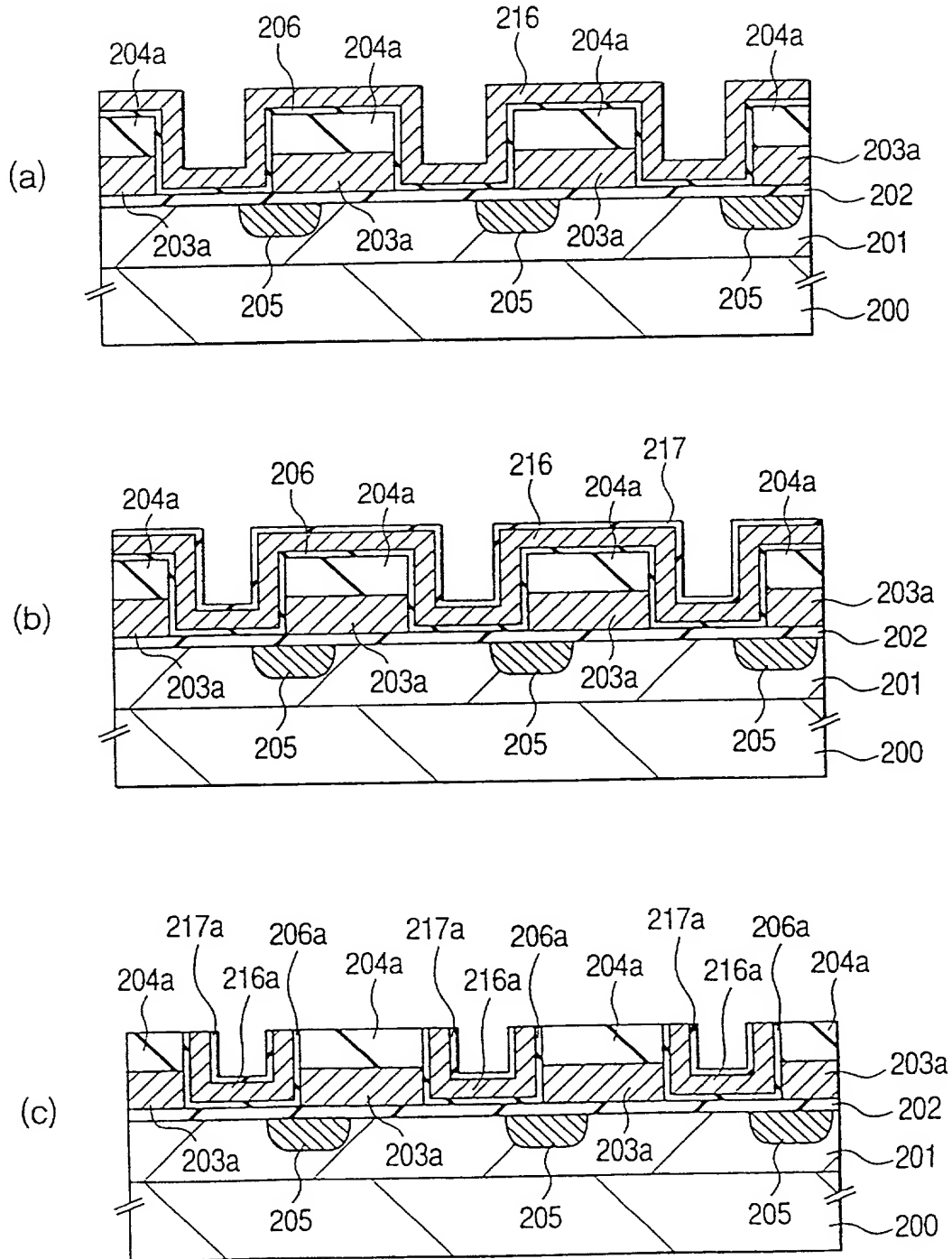


FIG. 11



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FIG. 12



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FIG. 13

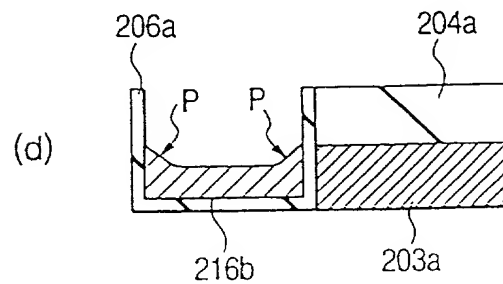
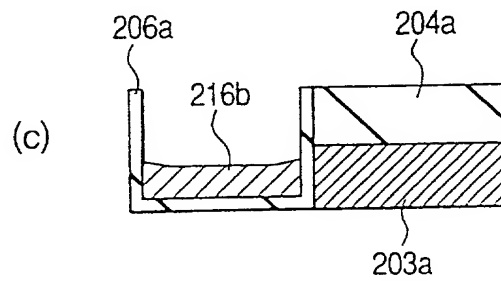
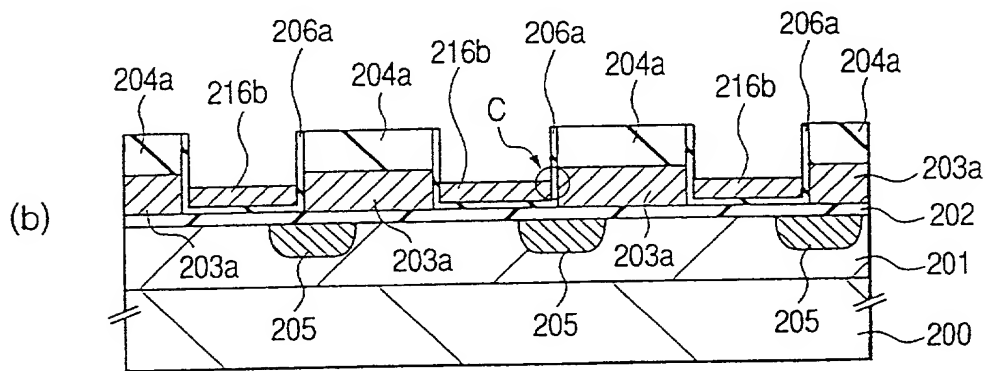
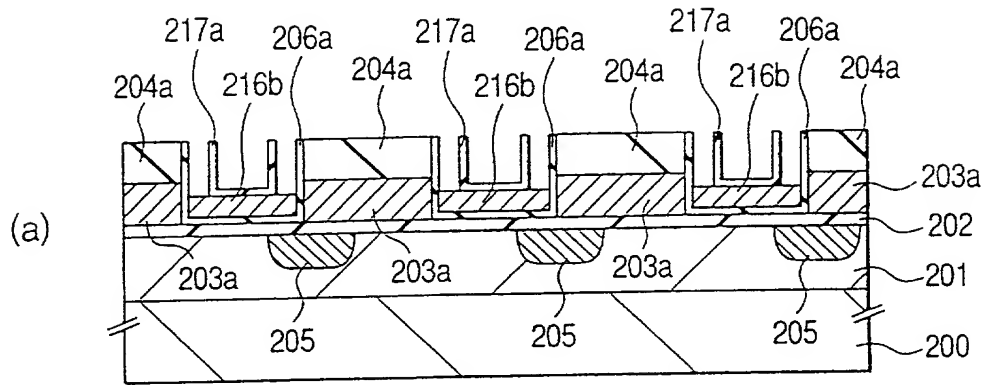


FIG. 14

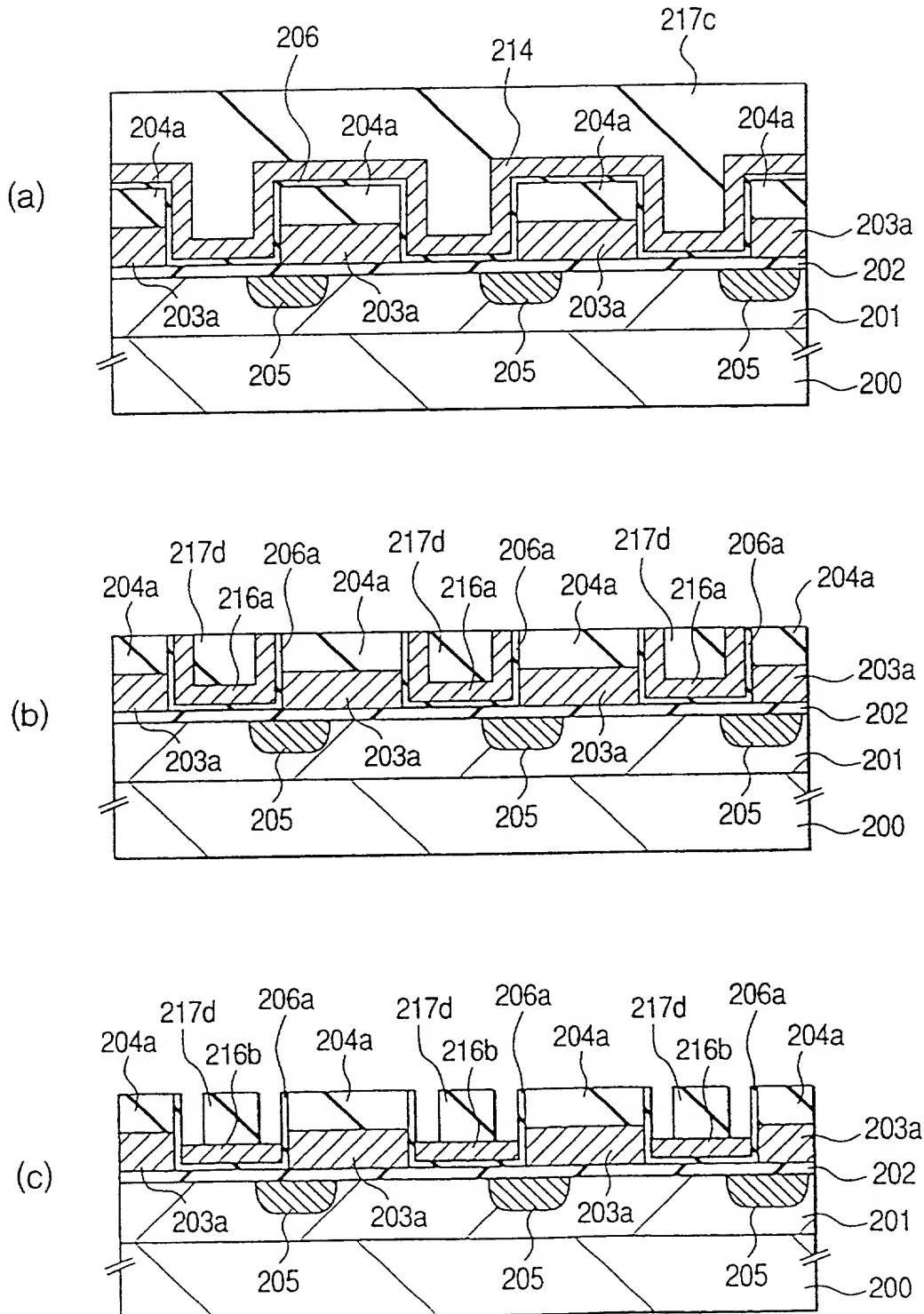


FIG. 15

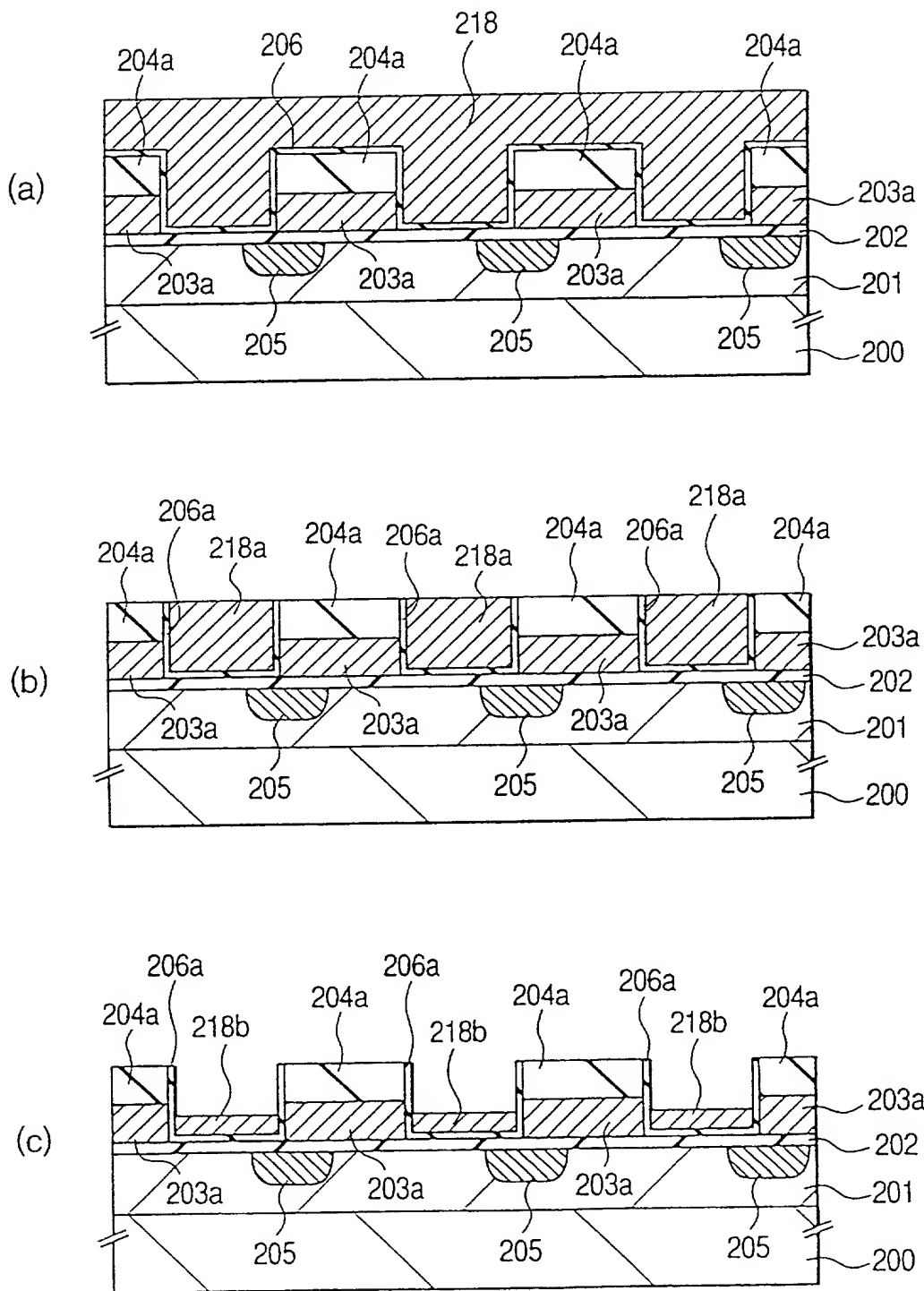


FIG. 16

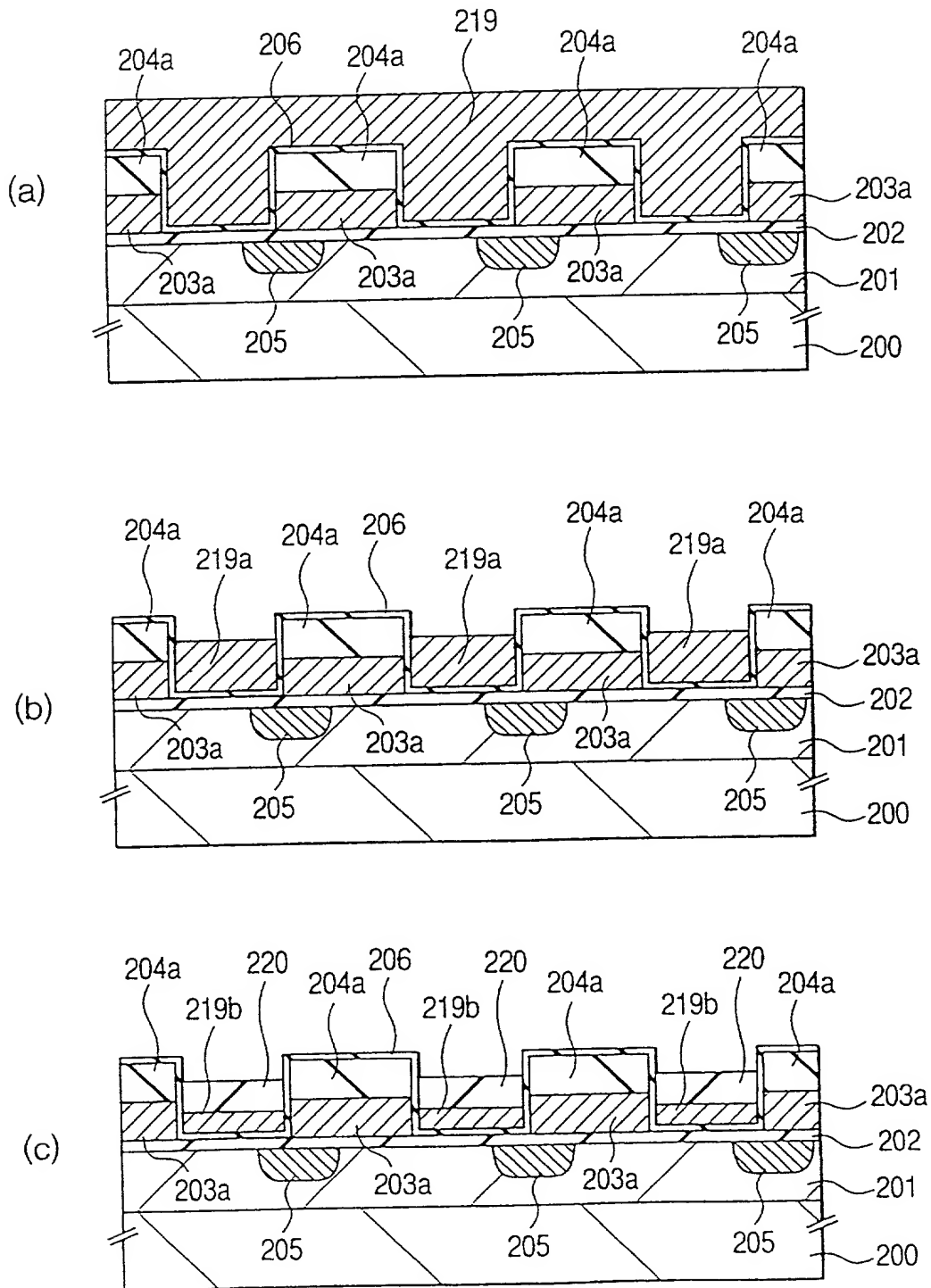


FIG. 17

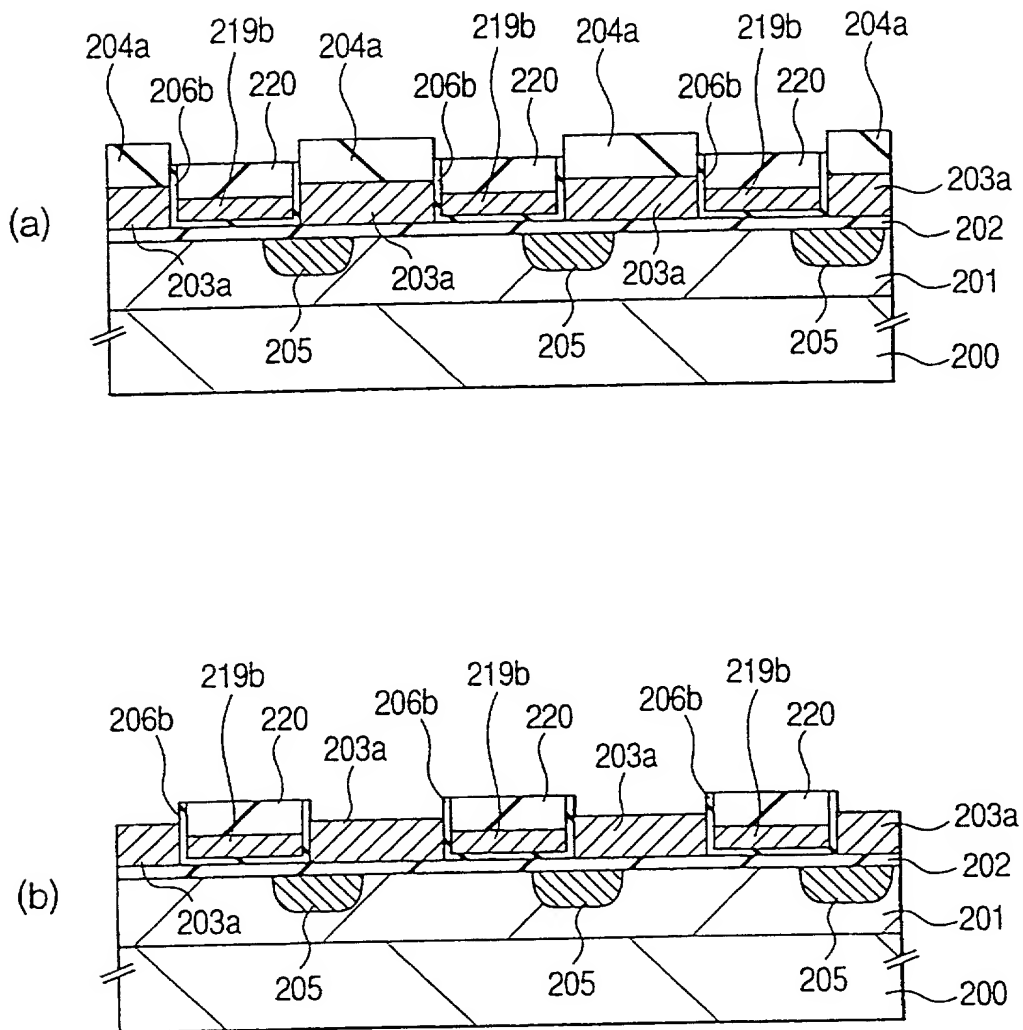


FIG. 18

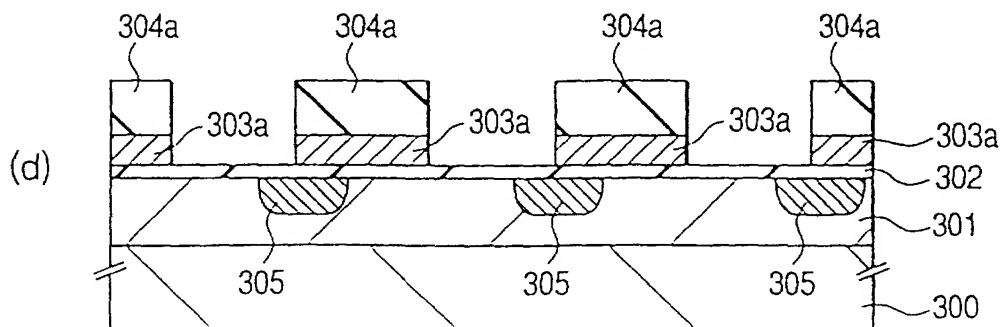
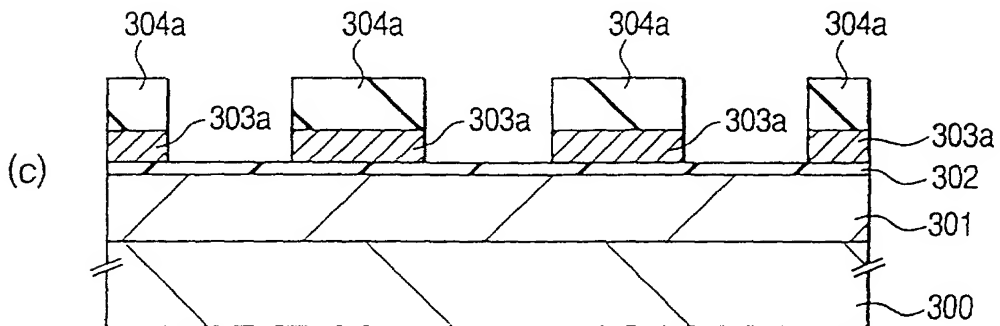
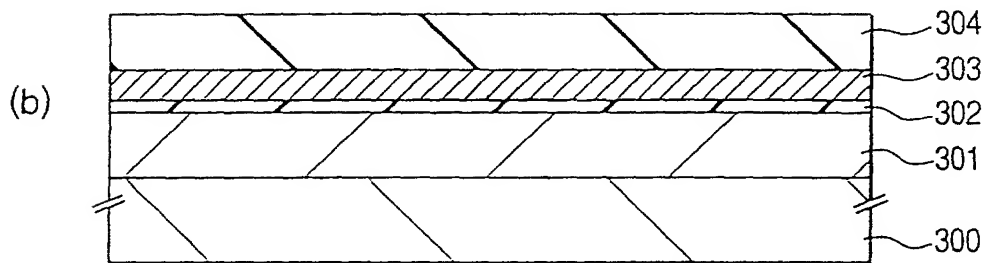
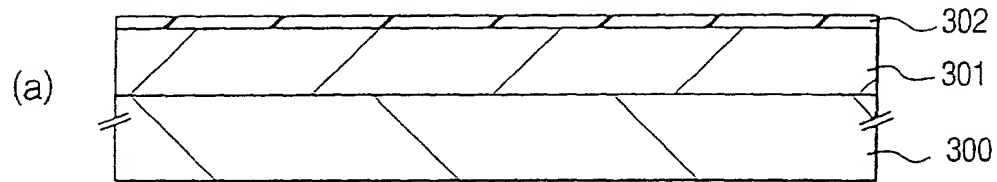


FIG. 19

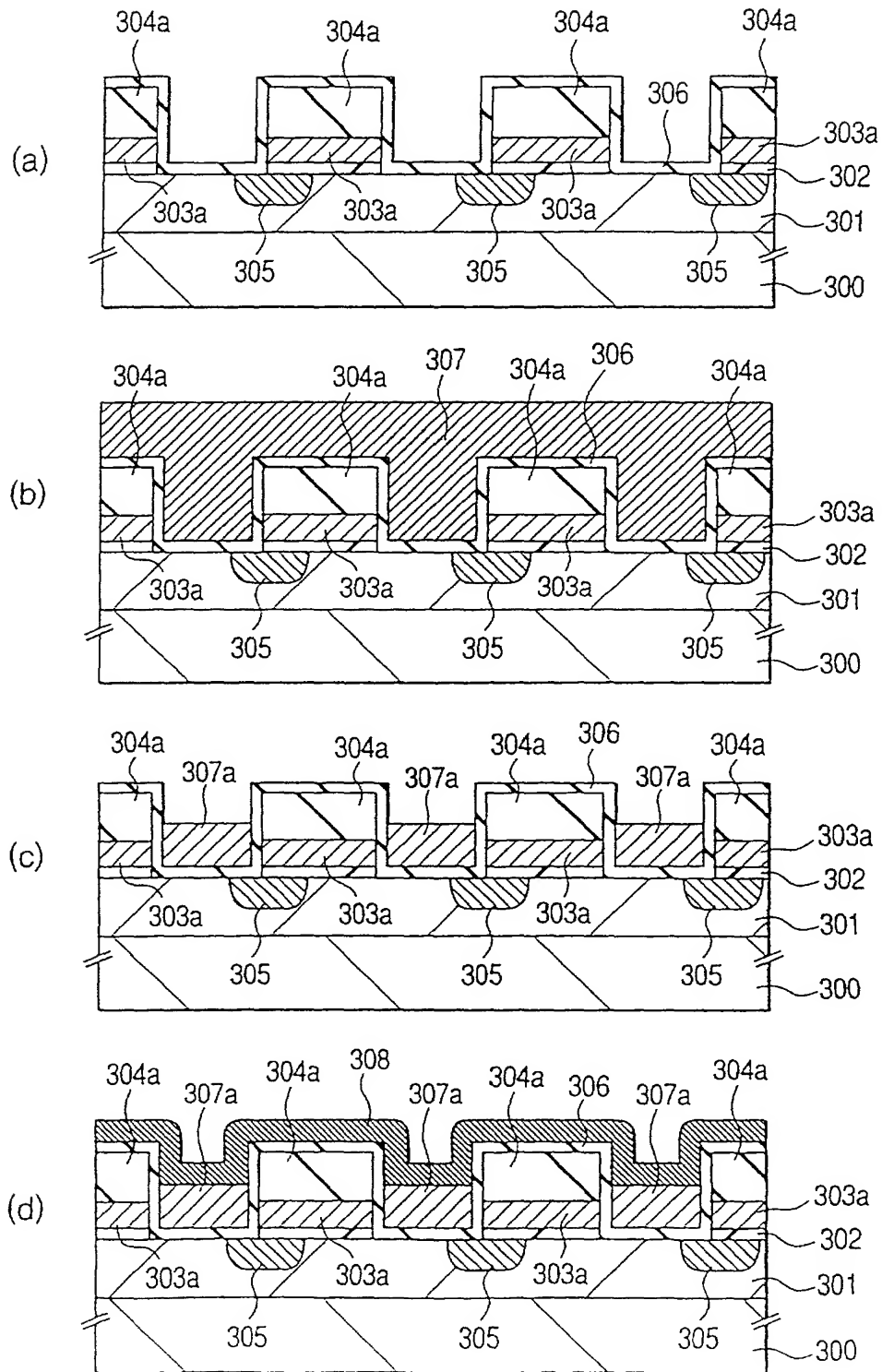


FIG. 20

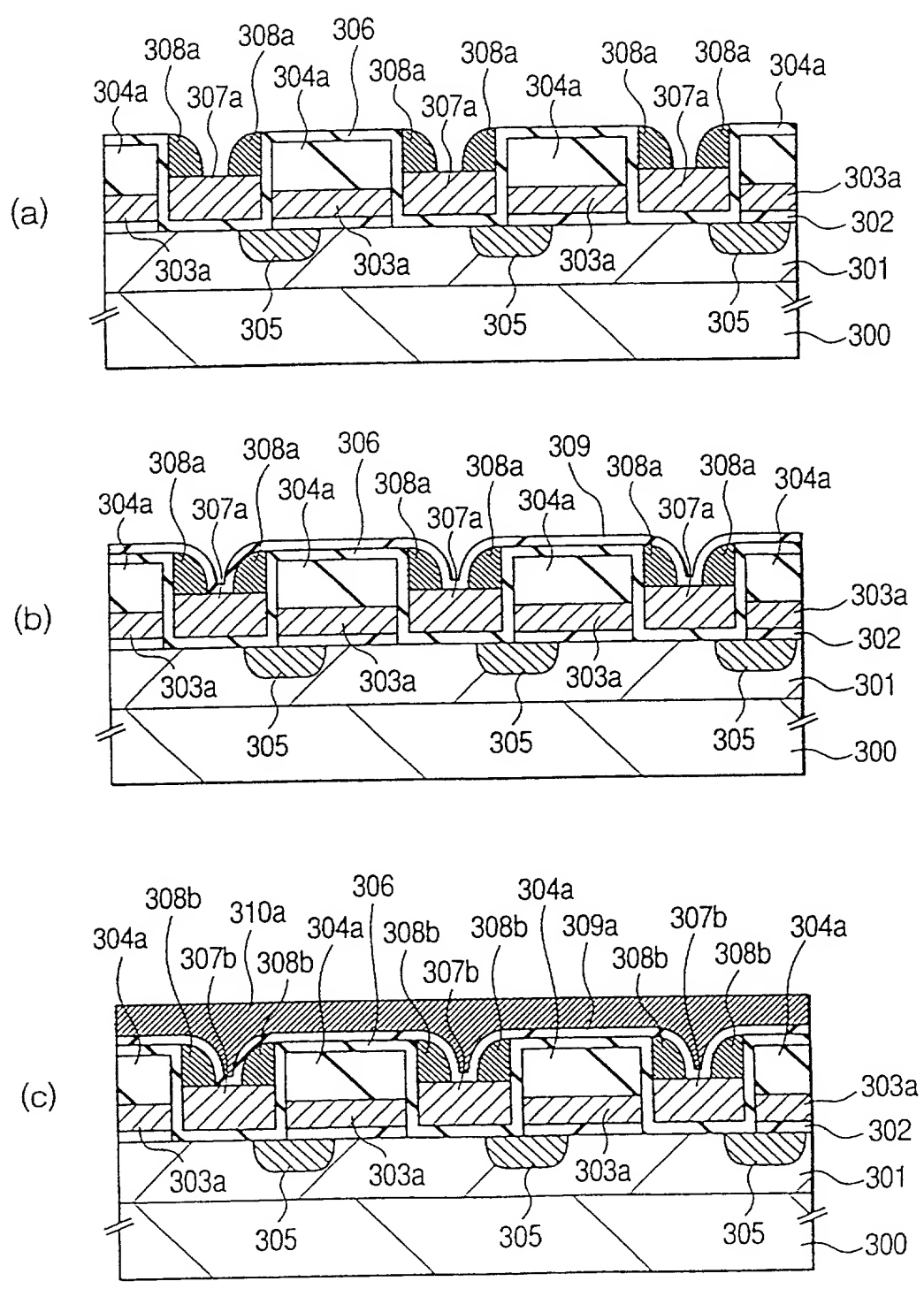


FIG. 22

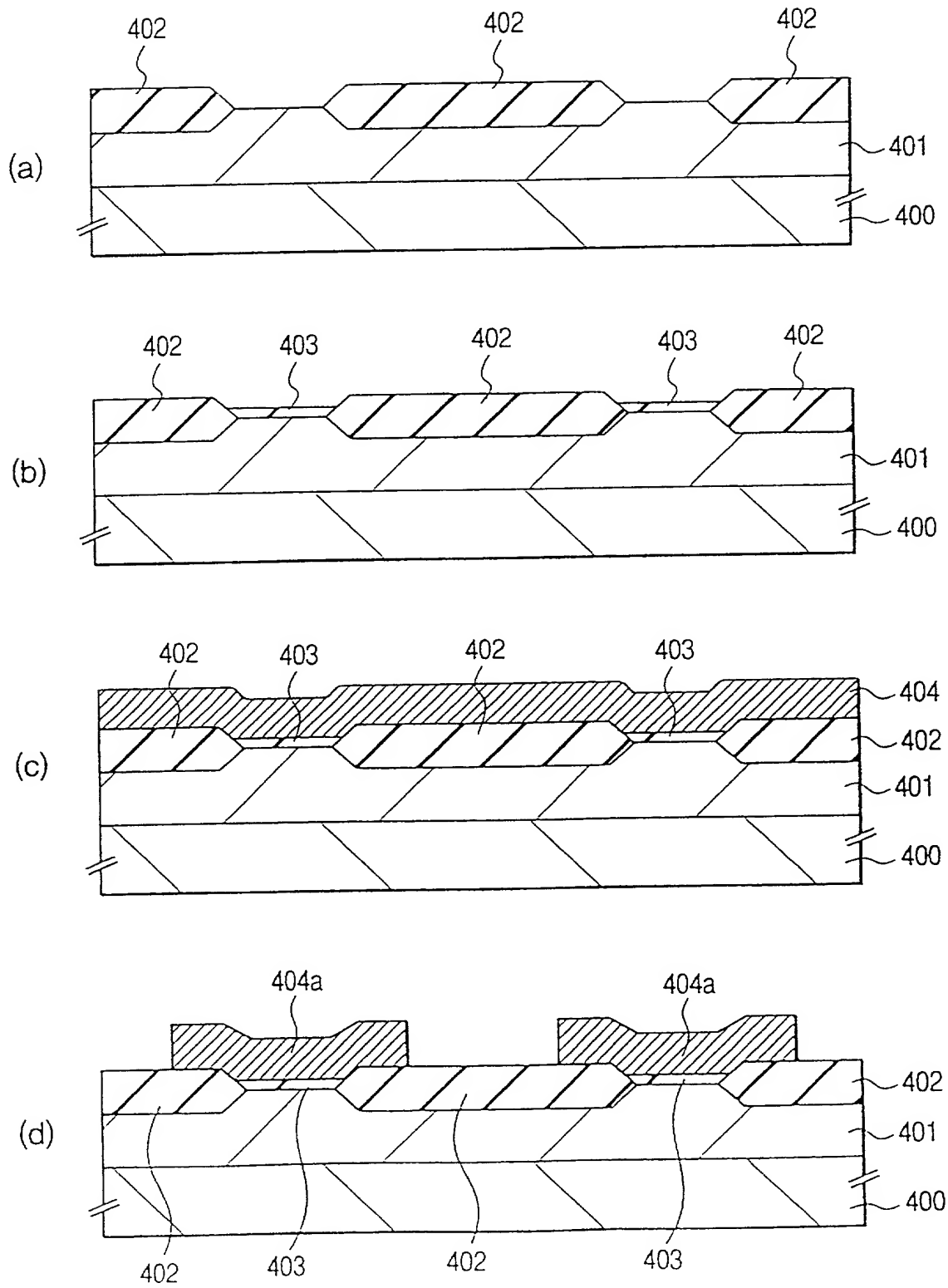


FIG. 23

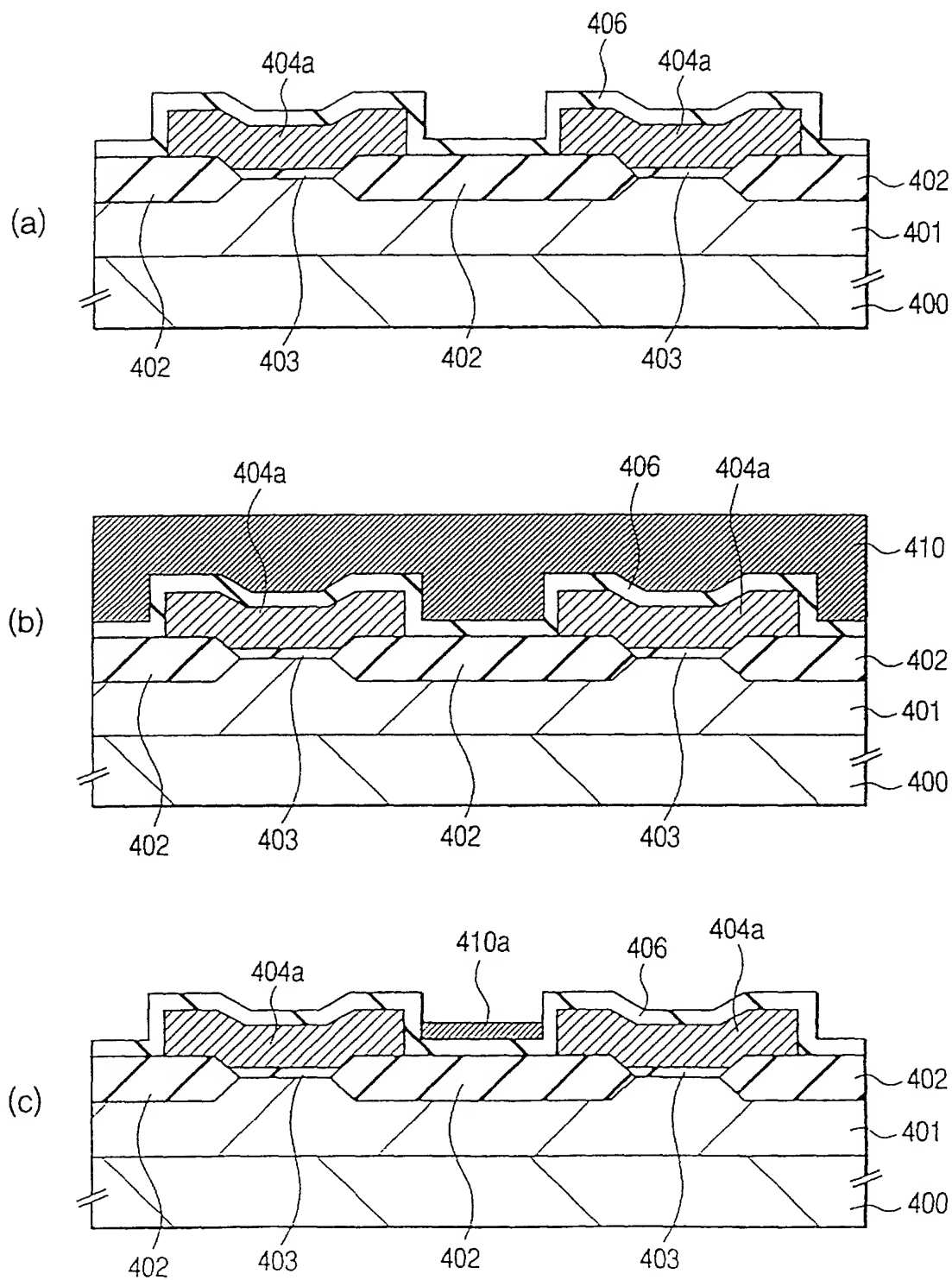
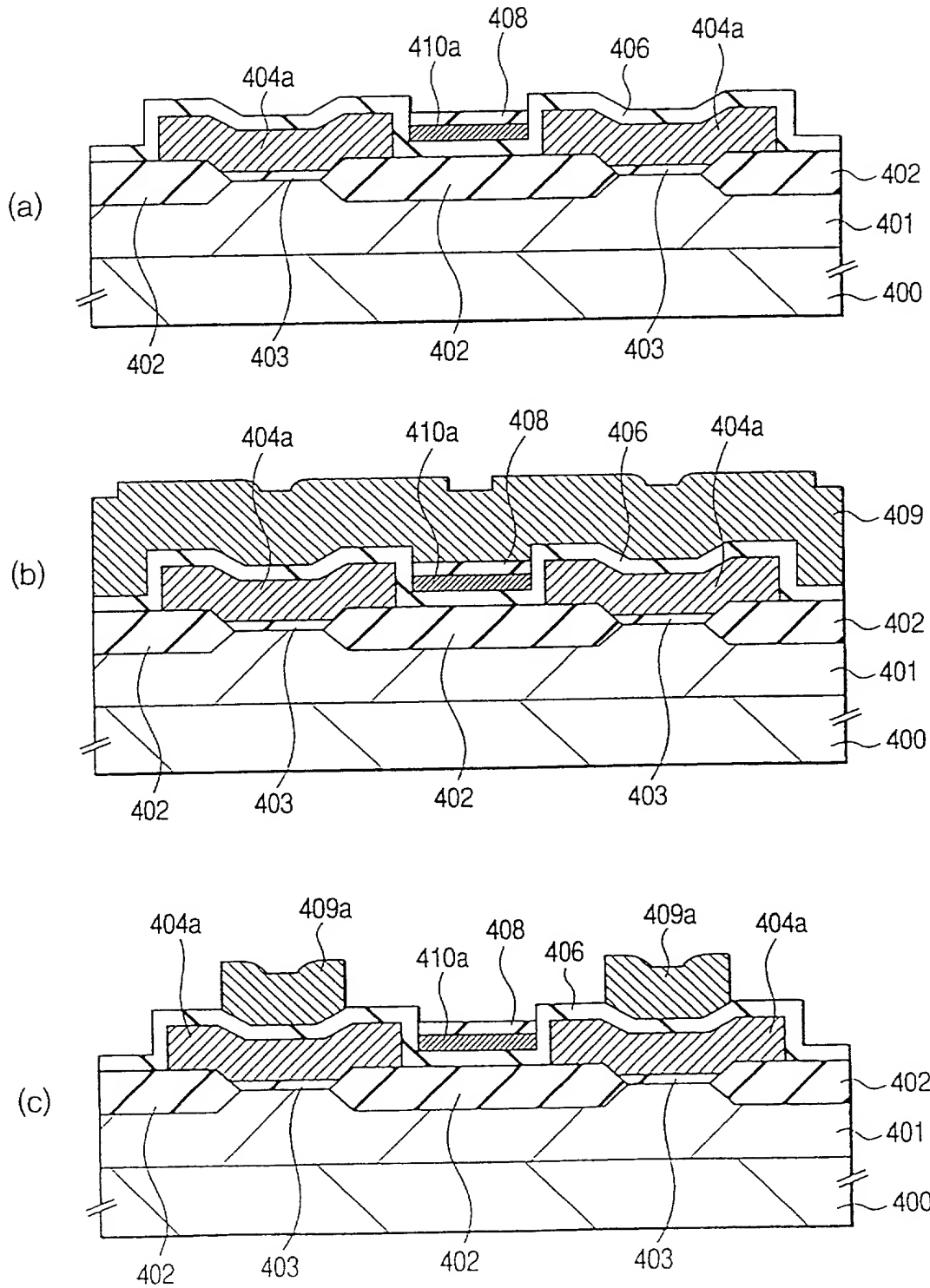


FIG. 24



CLAIMS

1. A process for producing a semiconductor integrated circuit device, which comprises a step of forming a first conduction type well in a silicon substrate; a step of forming a first pattern to act as floating gates on the silicon substrate through a first insulator film; a step of forming second conduction type semiconductor regions to act as sources/drains in the well; a step of forming a second insulator film covering the first pattern; a step of forming third gates in gaps formed in the first pattern through the second insulator film; a step of forming control gates on the upper surfaces of the floating gates and the third gates, the height of the upper surfaces of the third gates formed being lower than the height of the upper surface of the first pattern.

2. A process according to Claim 1, wherein the third gates are formed by any one of a first method of forming a polysilicon film completely filling the gaps, and then dry etching the polysilicon film, a second method of forming a polysilicon film completely filling the gaps, and then polishing the polysilicon film by chemical mechanical polishing, followed by dry etching, and a third method of forming a polysilicon film completely filling the gaps, then polishing the polysilicon film by chemical mechanical polishing, oxidizing the surface of the polysilicon film and selectively removing the oxidized parts.

3. A process according to Claim 1, wherein the third gates are formed by any one of a first method of forming a polysilicon film so as not to completely fill the gaps, then forming a photo resist film to fill the gap, and dry etching the photo resist film and the polysilicon film, a second method of forming a polysilicon film so as not to completely fill the gaps, then polishing the polysilicon film by chemical mechanical polishing, forming a photo resist to fill the gaps and dry etching the photo resist film and the polysilicon film, and a third method of forming a polysilicon film so as not to completely fill the gaps, then depositing a silicon oxide film to fill the gaps, polishing the silicon oxide film and the polysilicon film by chemical mechanical polishing, selectively removing the silicon oxide film in the gaps, forming a photo resist film to fill the gaps and dry etching the photo resist film and the polysilicon film.

4. A process according to Claim 3, wherein the dry etching of the photo resist and the polysilicon film is carried out at substantially equal etching speeds.

5. A process according to Claim 1, wherein the third gates are formed by a method of forming a polysilicon film so as not to completely fill the gaps, then forming a silicon oxide film on the polysilicon film, polishing the silicon oxide film and the polysilicon film by chemical mechanical polishing, dry

etching the polysilicon film and removing the silicon oxide film.

6. A process according to any one of Claims 3 to 5, wherein the thickness of the polysilicon film is made smaller than that of the first pattern to act as the floating gates.

7. A process for producing a semiconductor integrated circuit device, which comprises a step of forming a first conduction type well in a silicon substrate; a step of forming third gates on the silicon substrate through a second insulator film; a step of forming second conduction type semiconductor regions to act as sources/drains in the well; a step of forming a first insulator film covering the third gates; a step of forming a first pattern to act as floating gates in gaps formed between the third gates through the first insulator film; and a step of forming control gates on the upper surfaces of the floating gates and the third gates, the height of the upper surfaces of the third gates thus formed being made lower than that of the upper surface of the first pattern.

8. A process according to Claim 7, wherein the first pattern is formed by any one of a first method of forming a polysilicon film to completely fill the gaps, and then dry etching the polysilicon film, a second method of forming a polysilicon film to completely fill the gaps and then polishing the polysilicon film by chemical mechanical polishing, followed by dry etching;

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a third method of forming a polysilicon film so as not to completely fill the gaps and then polishing the polysilicon film by chemical mechanical polishing, a fourth method of forming a polysilicon film so as not to completely fill the gaps, then forming a photo resist film to fill the gaps and dry etching the photo resist film and the polysilicon film, and a fifth method of forming a polysilicon film so as not to completely fill the gaps, then depositing a silicon oxide film to fill the gaps and polishing the silicon oxide film and the polysilicon film by chemical mechanical polishing.

9. A process according to any one of Claims 1 to 8, wherein the third gates are self-aligned to the floating gates.

10. A process according to any one of Claims 1 to 8, wherein the floating gates are self-aligned to the third gates.

11. A semiconductor integrated circuit device, which comprises a first conduction type well formed on the main surface of a semiconductor substrate, second conduction type semiconductor regions formed in the well, first gates formed on the semiconductor substrate through a first insulator film, second gates formed on the first gates through a second insulator film and third gates formed through the first gates and a third insulator film, the third gates being formed to fill gaps between the first gates and the height of the

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surfaces of the third gates being made lower than that of the surfaces of the first gates.

12. A semiconductor integrated circuit device according to Claim 11, wherein the third gates are in any one of a first structure of erase gates, a second structure of gates controlling split channels, and a third structure having both functions of erase gates and gates controlling split channels.

13. A semiconductor integrated circuit device according to Claim 11 or 12, wherein the third insulator film is a nitrogen-introduced silicon oxide film.

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ADDITIONAL CLAIMS 14-39

14. A process for producing a semiconductor integrated circuit device, which comprises
- a step of forming a first conduction type well in a silicon substrate,
 - a step of forming a first pattern which is to become floating gates through a first insulator film on the semiconductor substrate,
 - a step of forming second conduction type semiconductor regions to act as sources/drains in the well,
 - a step of forming a second insulator film covering at least side faces of the first pattern and the semiconductor substrate surface between each first pattern,
 - a step of forming third gates in individual gaps formed by the first pattern so as to make individual side faces of the third gates opposed to side faces of neighboring first pattern through the second insulator film and to make bottom sides of the third gates opposed to a surface of the semiconductor substrate through the second insulator film by depositing a third gate material film, followed by removing the material film above each first pattern, and
 - a step of forming the floating gates and forming control gates on the third gates.

15. A process for producing a semiconductor integrated circuit device according to claim 14, wherein the upper ends of side faces of the third gates are formed lower than the upper ends of side faces of the first pattern which is to become the floating gates opposed to the side faces of the third gates.

16. A process for producing a semiconductor integrated circuit device according to claim 15, wherein the third gates are obtained by forming a polycrystalline silicon film for completely filling the gaps, and dry etching

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the polycrystalline silicon film.

17. A process for producing a semiconductor integrated circuit device according to claim 15, wherein the third gates are obtained by forming a polycrystalline silicon film for completely filling the gaps, polishing the polycrystalline silicon film by a chemical mechanical polishing method, followed by dry etching.

18. A process for producing a semiconductor integrated circuit device according to claim 15, wherein the third gates are obtained by forming a polycrystalline silicon film for completely filling the gaps, polishing the polycrystalline silicon film by a chemical mechanical polishing method, oxidizing a surface of the polycrystalline silicon film, and selectively removing the oxidized portion thus obtained.

19. A process for producing a semiconductor integrated circuit device according to claim 15, wherein the third gates are obtained by forming a polycrystalline silicon film so as not to completely fill the gaps, forming a photo resist film for filling the gaps, and subjecting the photo resist film and the polycrystalline silicon film to dry etching.

20. A process for producing a semiconductor integrated circuit device according to claim 15, wherein the third gates are obtained by forming a polycrystalline silicon film so as not to completely fill the gaps, polishing the polycrystalline silicon film by a chemical mechanical polishing method, forming a photo resist film for filling the gaps, and subjecting the photo resist film and the polycrystalline silicon film to dry etching.

21. A process for producing a semiconductor

integrated circuit device according to claim 15, wherein the third gates are obtained by forming a polycrystalline silicon film so as not to completely fill the gaps, depositing a silicon oxide film for filling the gaps, polishing the silicon oxide film and the polycrystalline silicon film by a chemical mechanical polishing method, selectively removing the silicon oxide film in the gaps, forming a photo resist film for filling the gaps, and subjecting the photo resist film and the polycrystalline silicon film to dry etching.

22. A process for producing a semiconductor integrated circuit device according to any one of claims 19 to 21, wherein the dry etching of the photo resist film and that of the polycrystalline silicon film are conducted at almost the same etching speed.

23. A process for producing a semiconductor integrated circuit device according to claim 15, wherein the third gates are obtained by forming a polycrystalline silicon film so as not to completely fill the gaps, forming a silicon oxide film on the polycrystalline silicon film, polishing the silicon oxide film and the polycrystalline silicon film by a chemical mechanical polishing method, dry etching the polycrystalline silicon film, and removing the silicon oxide film.

24. A process for producing a semiconductor integrated circuit device according to any one of claims 19 to 23, wherein the polycrystalline silicon film has a film thickness thinner than that of the first pattern which becomes the floating gates.

25. A process for producing a semiconductor integrated circuit device, which comprises
a step of forming a first conduction type well

in a silicon substrate,

a step of forming a plurality of third gates through a second insulator film on the semiconductor substrate,

a step of forming second conduction type semiconductor regions to act as sources/drains in the well,

a step of forming a first insulator film covering at least side faces of the third gates and the semiconductor substrate surface between each third gates,

a step of forming a first pattern which is to become floating gates in individual gaps formed by the third gates so as to make individual side faces of the first pattern opposed to side faces of neighboring third gates through the first insulator film and to make a bottom side of the first pattern opposed to a surface of the semiconductor substrate through the first insulator film by depositing a floating gate material film, followed by removing the material film above each third gate, and

a step of forming the floating gates and forming control gates on the third gates.

26. A process for producing a semiconductor integrated circuit device according to claim 25, wherein the upper ends of side faces of the third gates are formed lower than the upper end of side face of the first pattern which is to become the floating gates opposed to the side faces of the third gates.

27. A process for producing a semiconductor integrated circuit device according to claim 26, wherein the first pattern is obtained by forming a polycrystalline silicon film for completely filling the gaps, and dry etching the polycrystalline silicon film.

28. A process for producing a semiconductor integrated circuit device according to claim 26, wherein the first pattern is obtained by forming a polycrystalline

silicon film for completely filling the gaps, polishing the polycrystalline silicon film by a chemical mechanical polishing method, followed by dry etching.

29. A process for producing a semiconductor integrated circuit device according to claim 26, wherein the first pattern is obtained by forming a polycrystalline silicon film so as not to completely fill the gaps, and polishing the polycrystalline silicon film by a chemical mechanical polishing method.

30. A process for producing a semiconductor integrated circuit device according to claim 26, wherein the first pattern is obtained by forming a polycrystalline silicon film so as not to completely fill the gaps, forming a photo resist film for filling the gaps, and subjecting the photo resist film and the polycrystalline silicon film to dry etching.

31. A process for producing a semiconductor integrated circuit device according to claim 26, wherein the first pattern is obtained by forming a polycrystalline silicon film so as not to completely fill the gaps, depositing a silicon oxide film for filling the gaps, and polishing the silicon oxide film and the polycrystalline silicon film by a chemical mechanical polishing method.

32. A process for producing a semiconductor integrated circuit device according to any one of claims 14 to 31, wherein the third gates are formed as self-aligned to the floating gates.

33. A process for producing a semiconductor integrated circuit device according to any one of claims 14 to 31, wherein the floating gates are formed as self-aligned to the third gates.

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34. A semiconductor integrated circuit device comprising a first conduction type well formed on a major surface of a semiconductor substrate, second conduction type semiconductor regions formed in the well, first gates formed on the semiconductor substrate through a first insulator film, second gates formed on the first gates through a second insulator film, and third gates formed through the first gates and a third insulator film, wherein the third gates are formed by filling gaps in the first gates so as to make side faces of the third gates opposed to neighboring side faces of the first gates through the third insulator film and extended in an almost vertical direction to the direction of extended second gates.

35. A semiconductor integrated circuit device according to claim 34, wherein the third gates have upper ends of side faces lower than upper ends of side faces of the first gates opposed to the side faces of the third gates.

36. A semiconductor integrated circuit device according to claim 35, wherein the third gates are erase gates.

37. A semiconductor integrated circuit device according to claim 35, wherein the third gates are gates for controlling split channels.

38. A semiconductor integrated circuit device according to claim 35, wherein the third gates have functions of both erase gates and gates for controlling split channels.

39. A semiconductor integrated circuit device according to any one of claims 35 to 38, wherein the third insulator film is a nitrogen-introduced silicon oxide film.

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FIG. 1

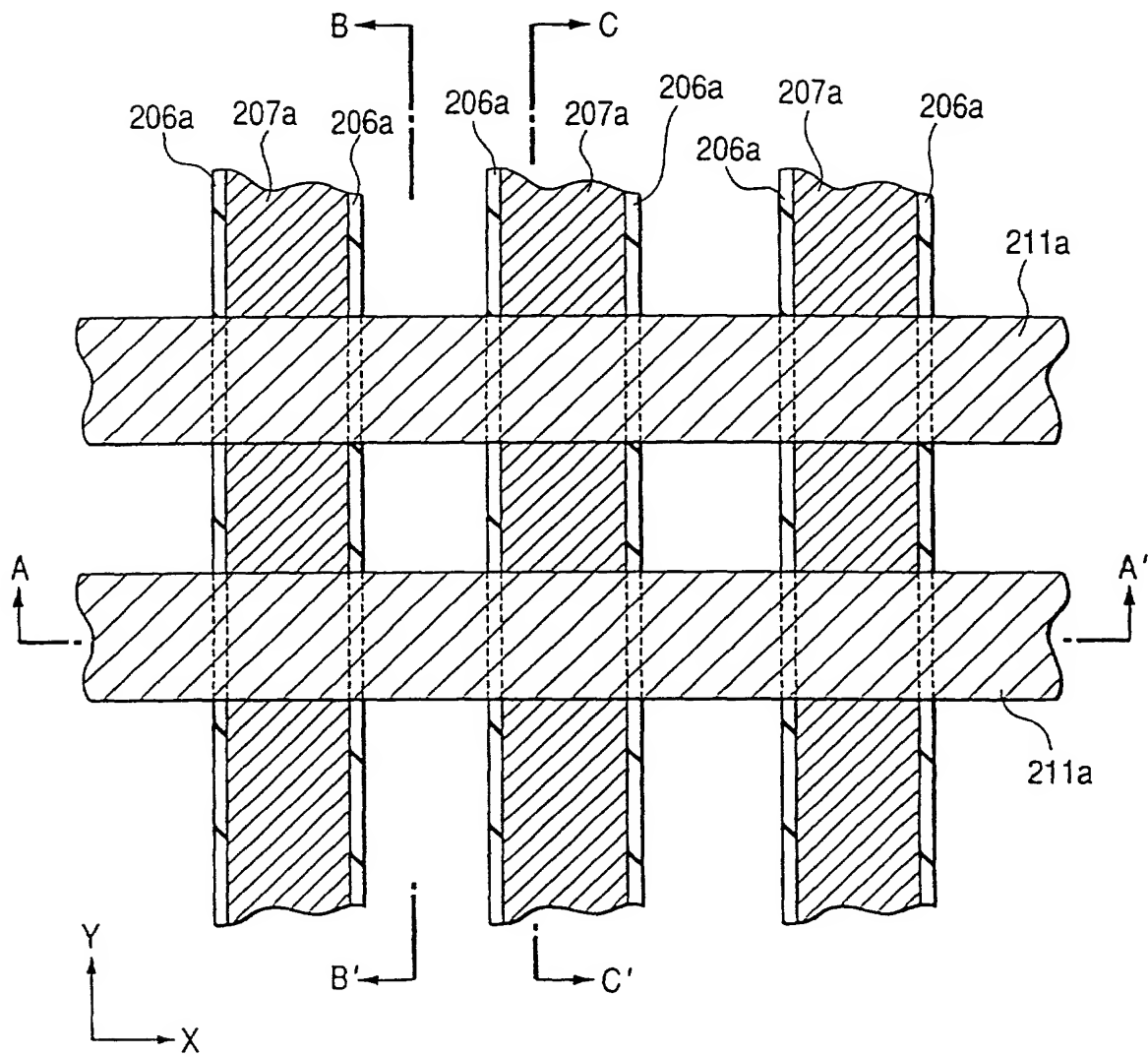
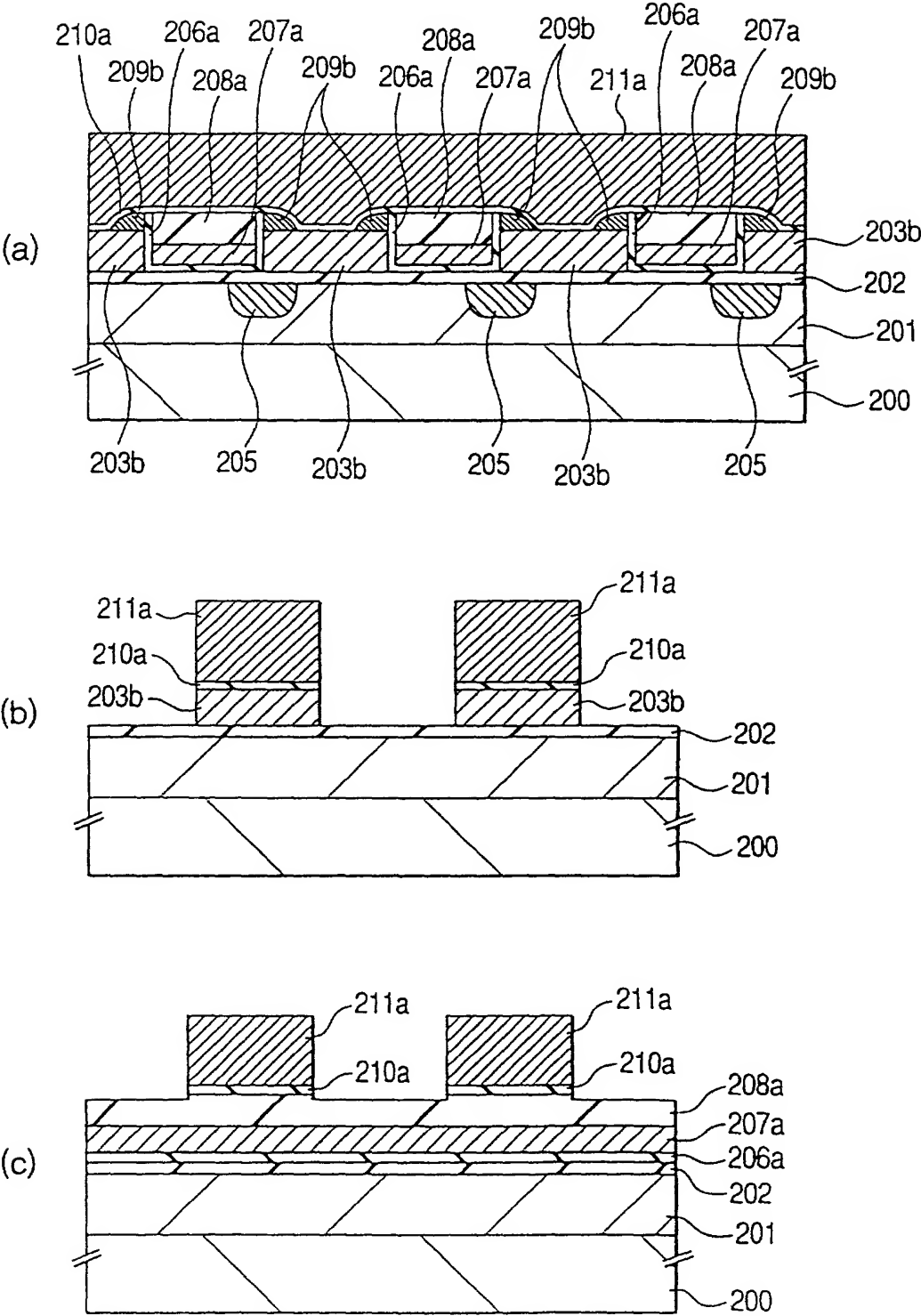


FIG. 2



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FIG. 3

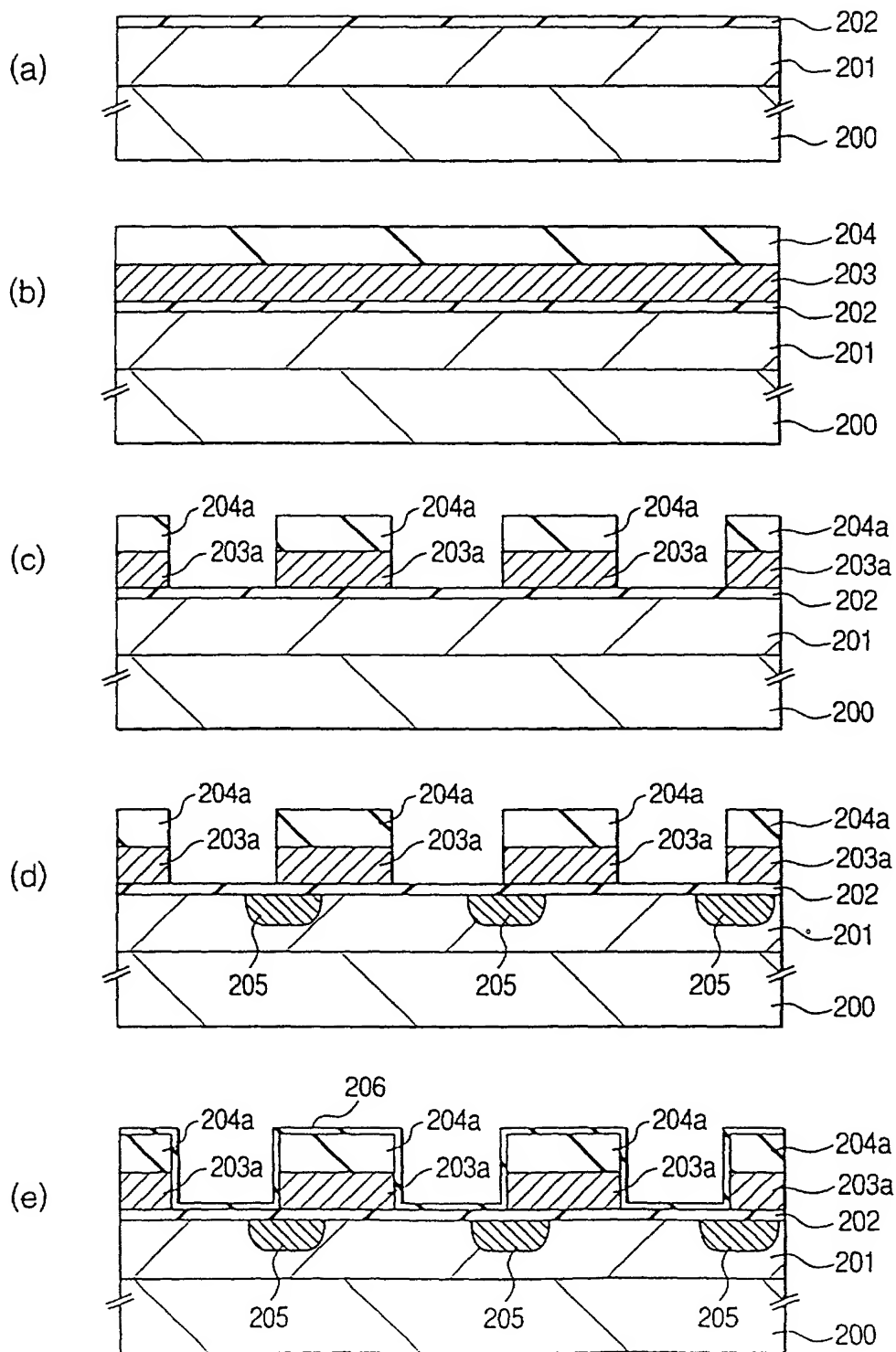
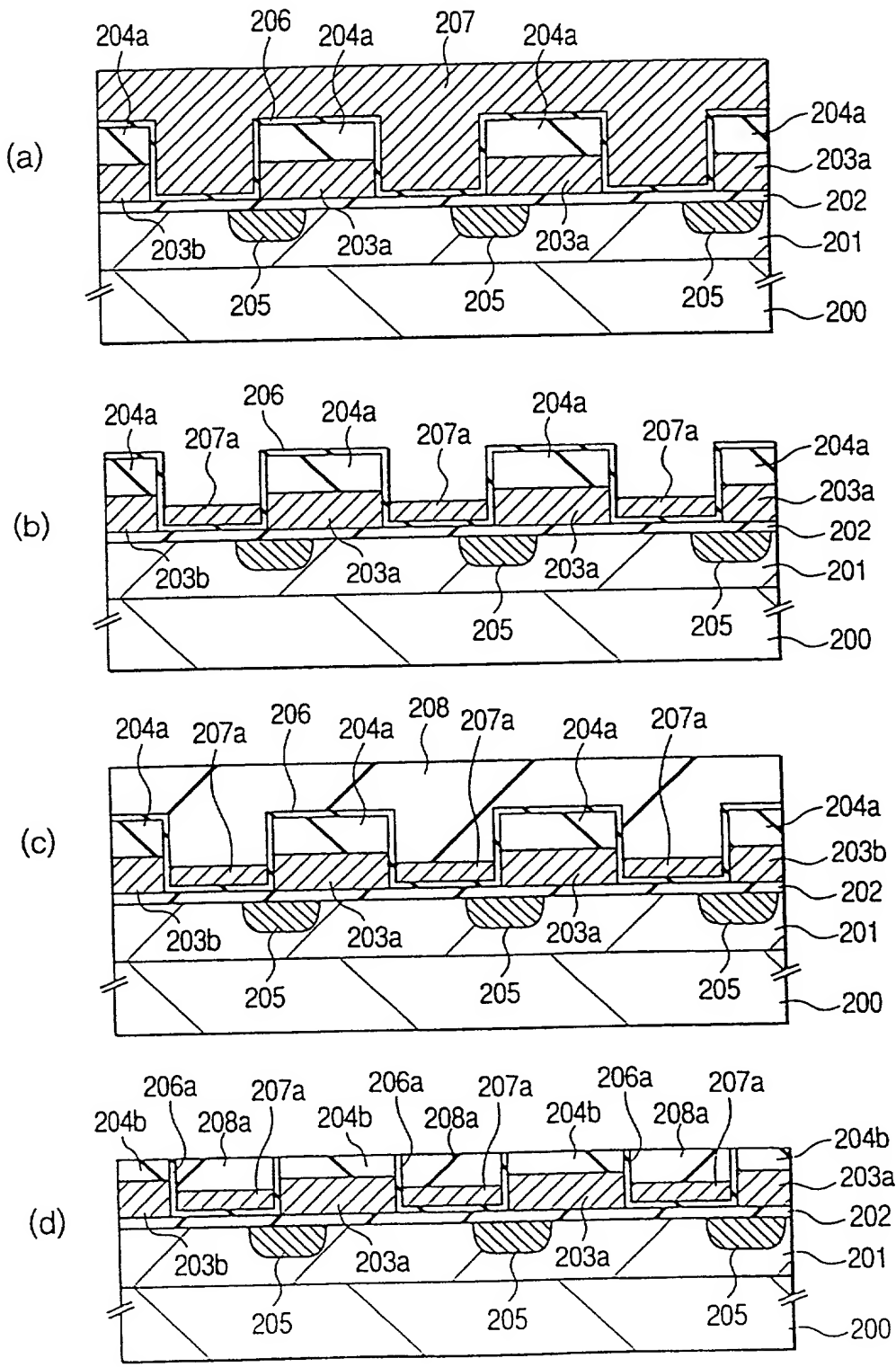
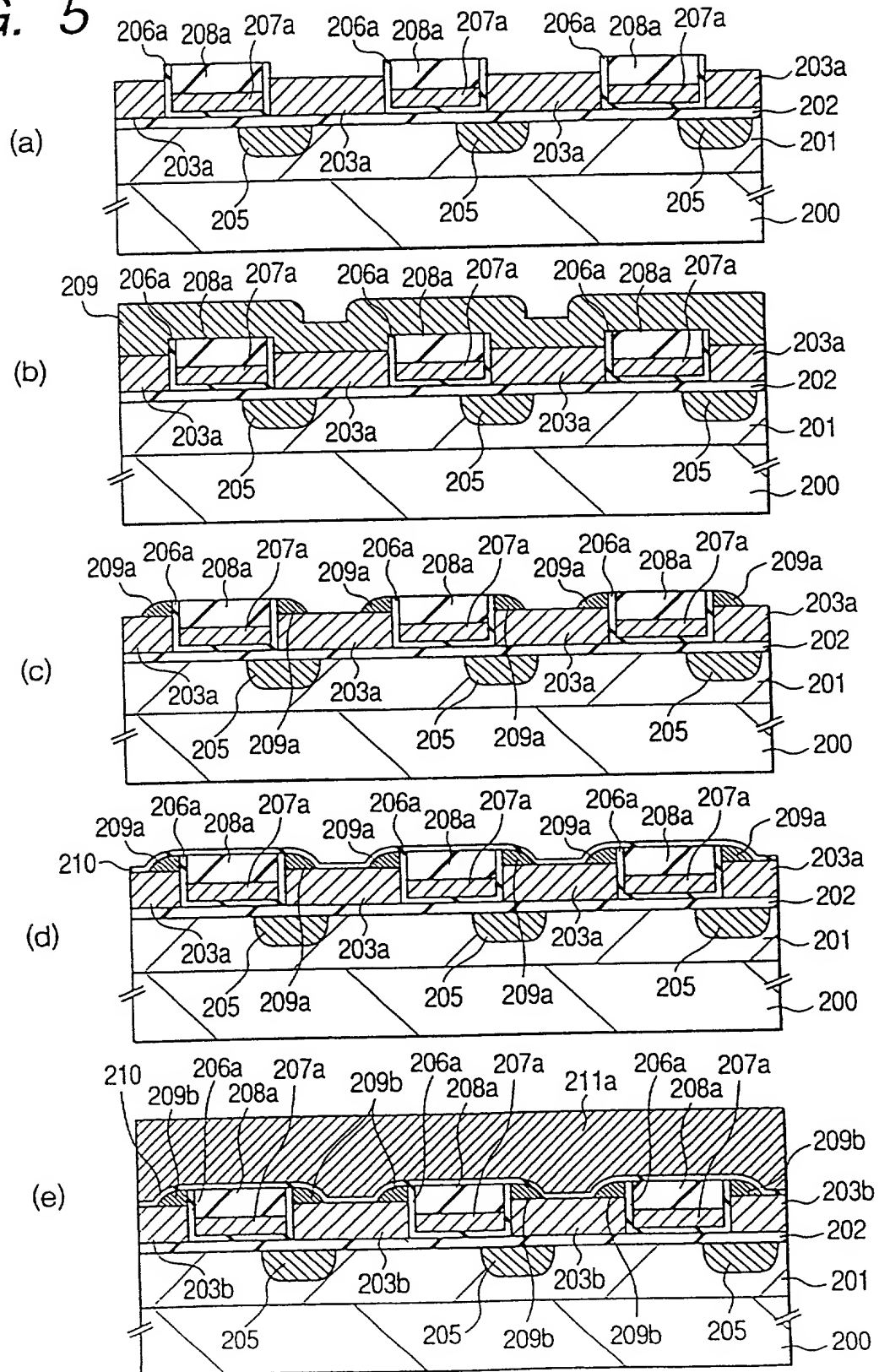


FIG. 4



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FIG. 5



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FIG. 6

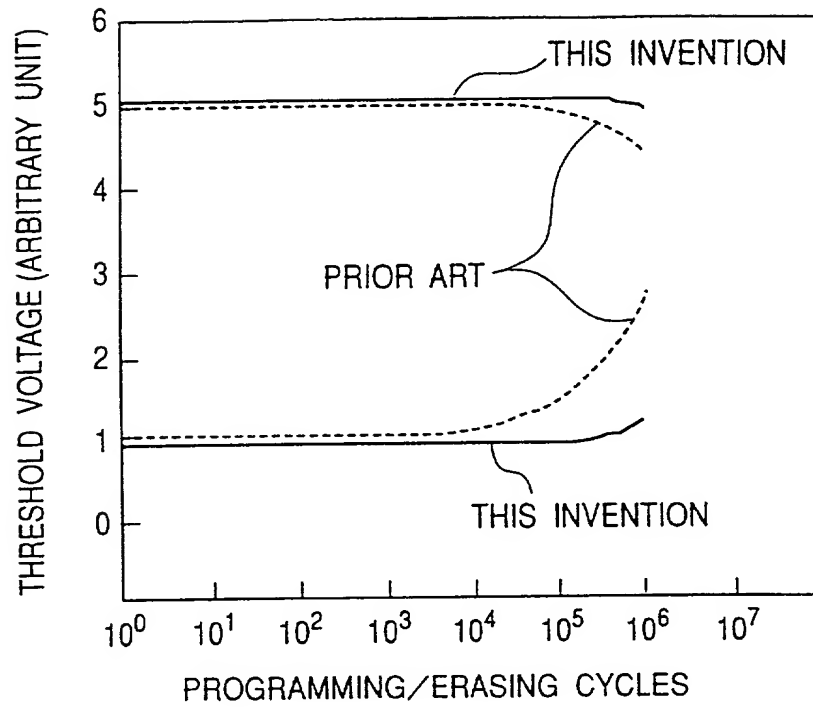
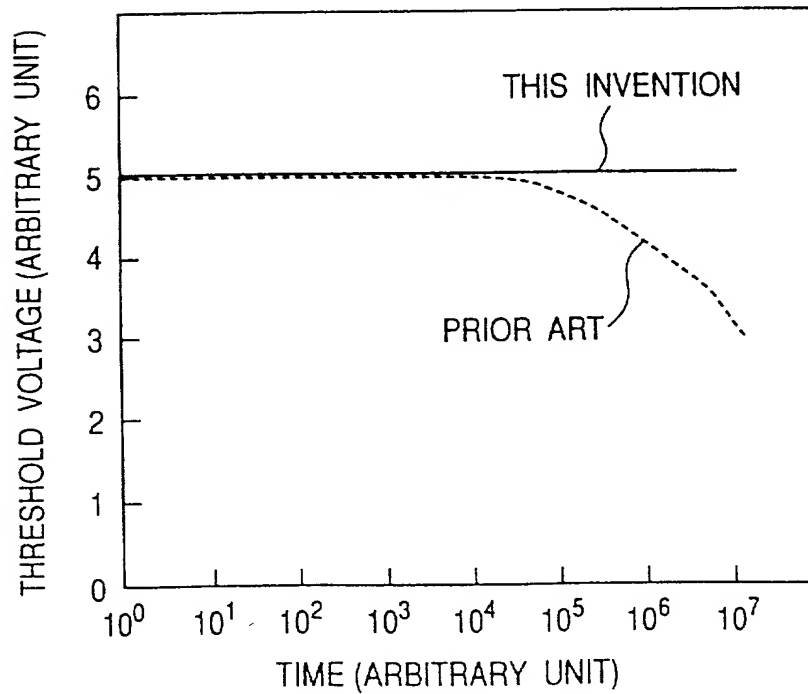
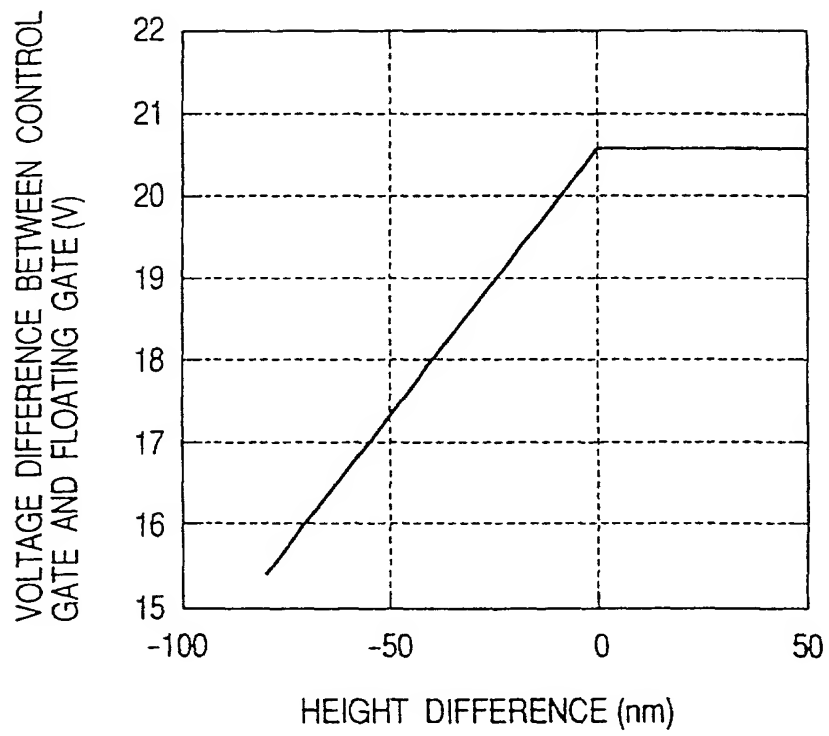


FIG. 7



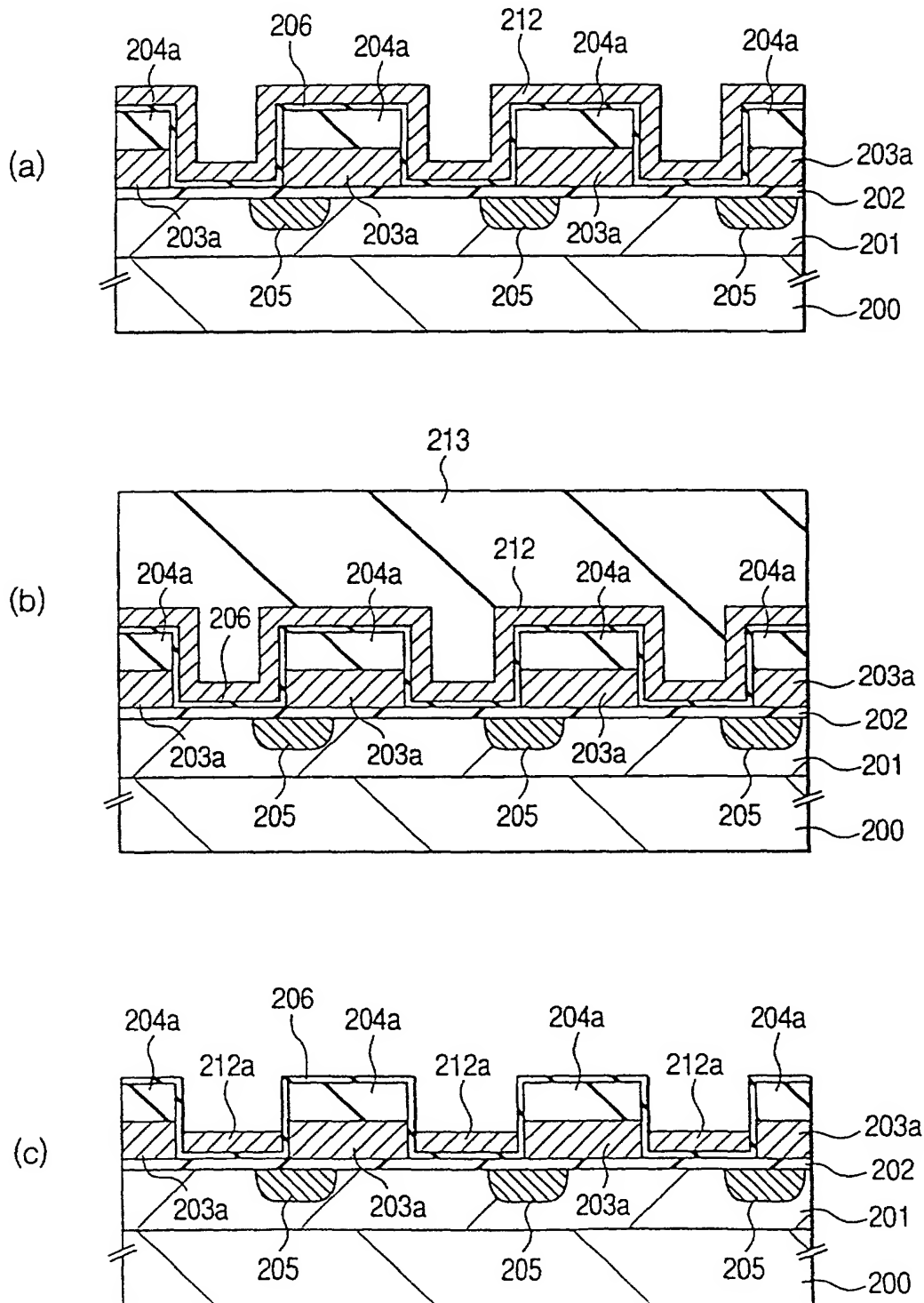
7/23

FIG. 8



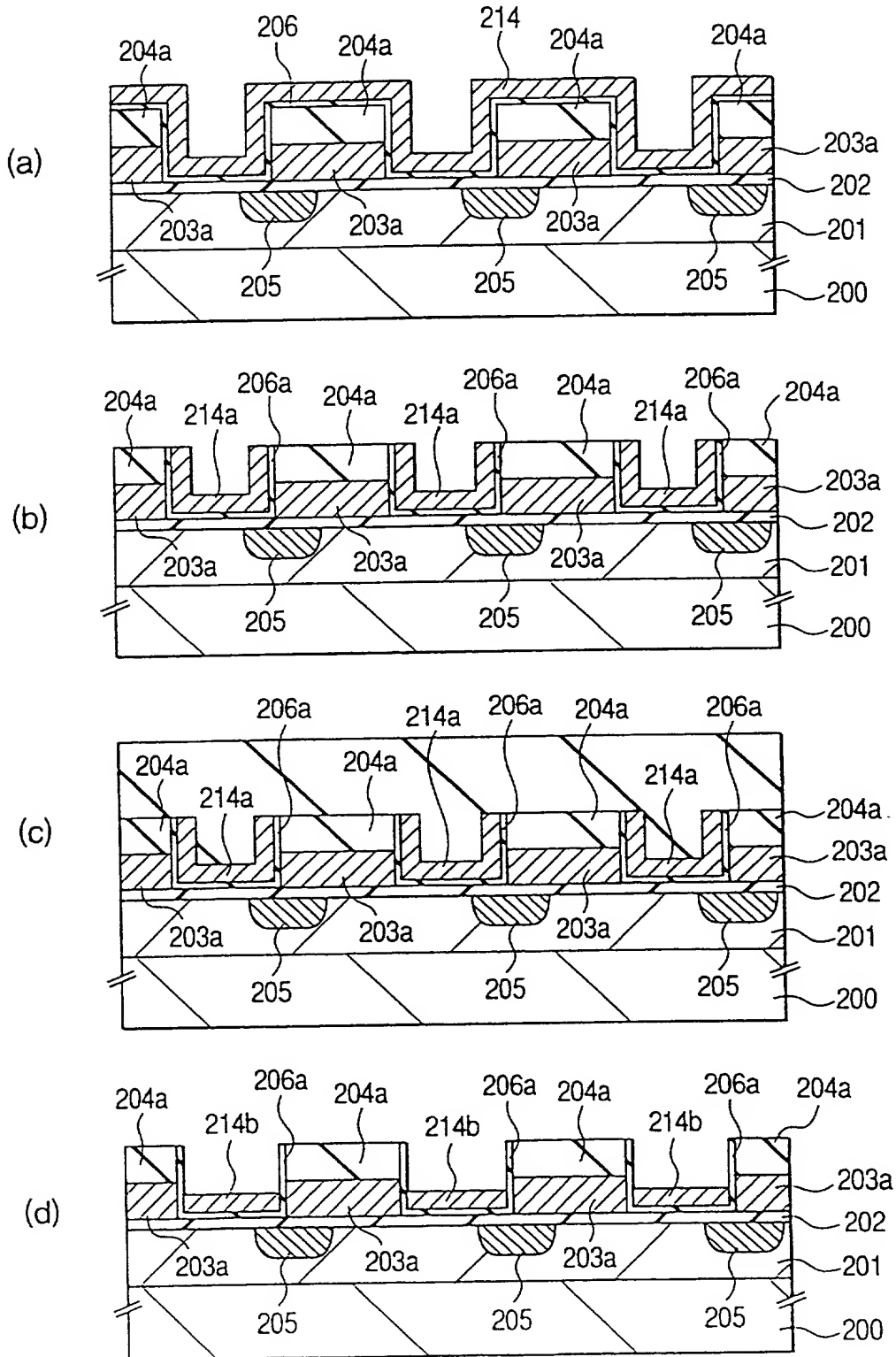
8/23

FIG. 9



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FIG. 10



200 201 202 203a 204a 205 206 206a 214a 214b

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FIG. 11

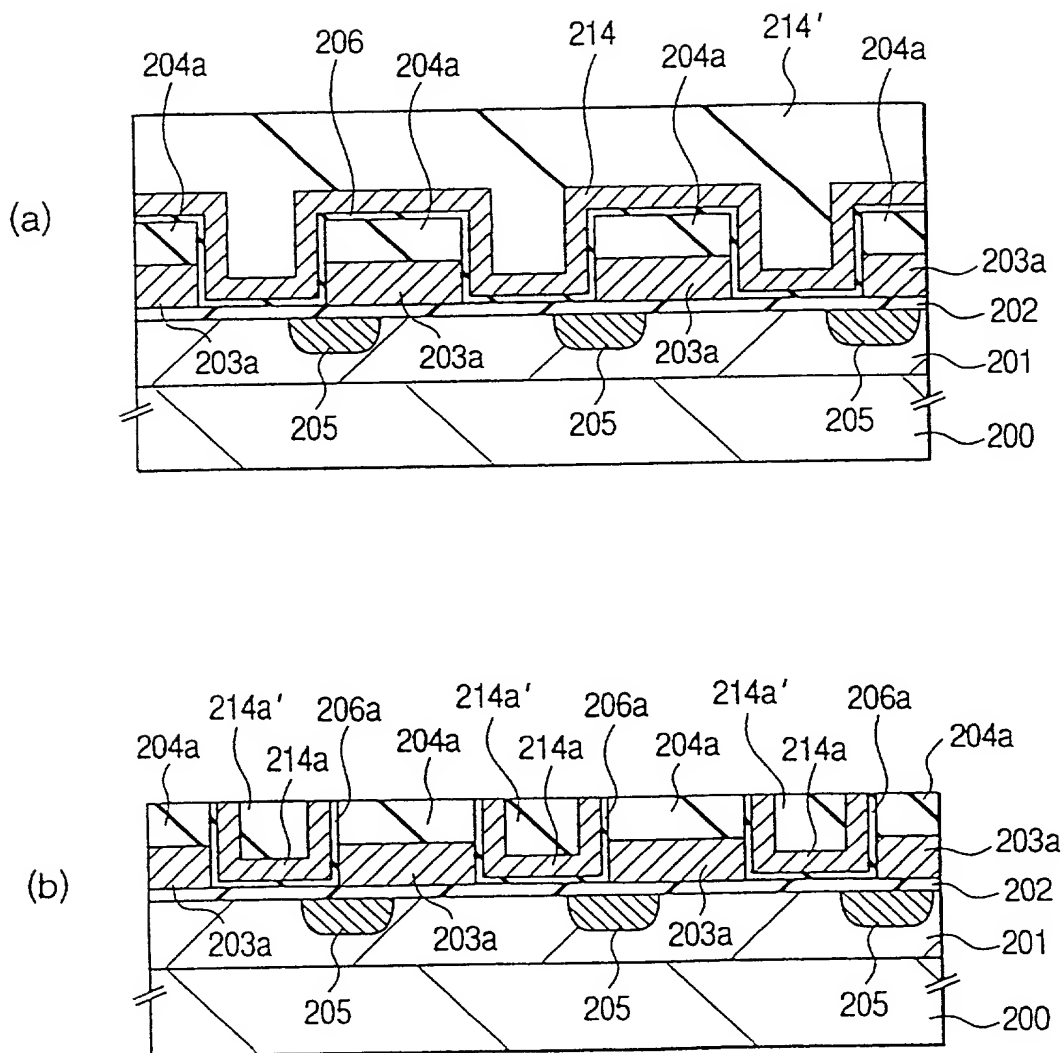
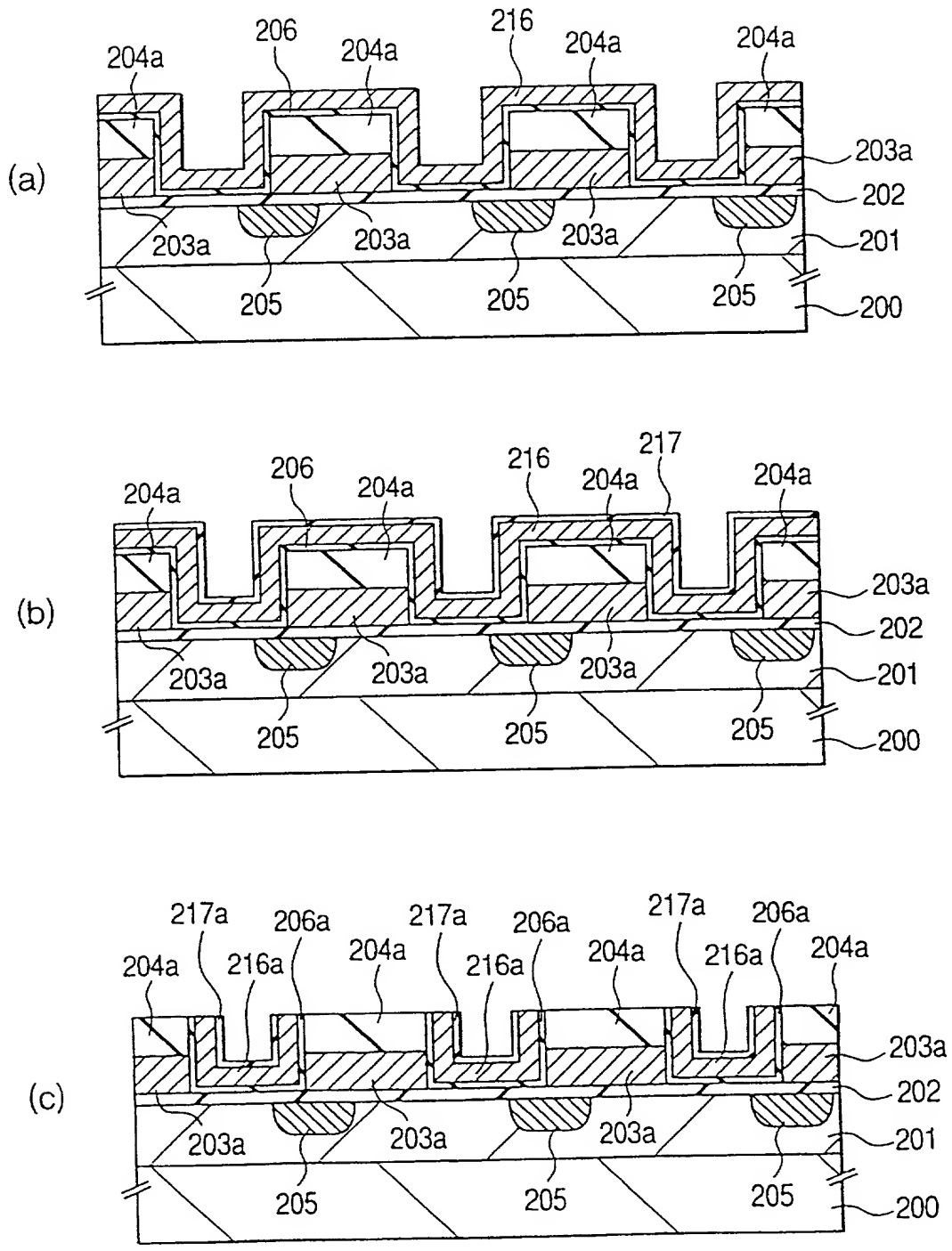


FIG. 12



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FIG. 13

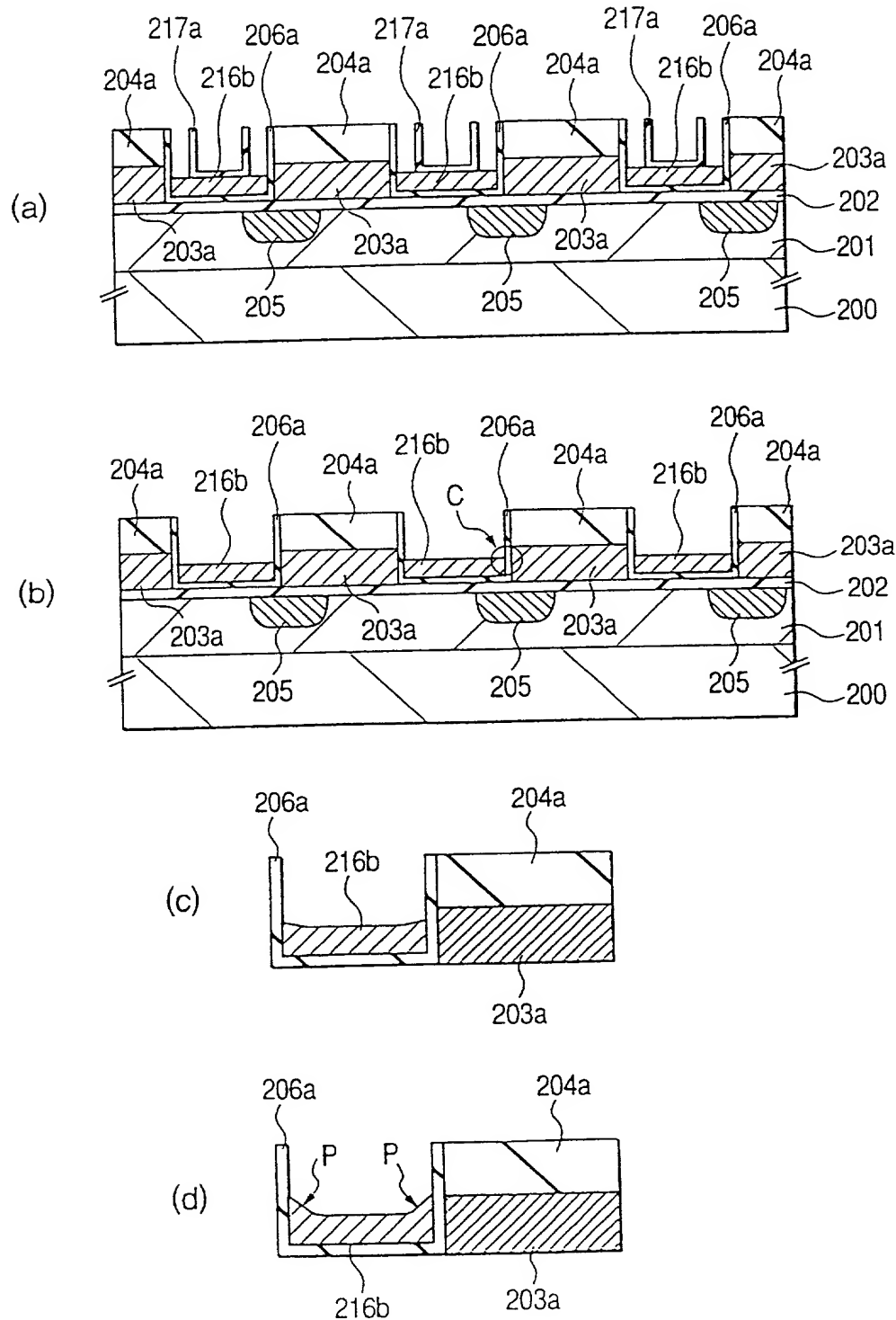


FIG. 14

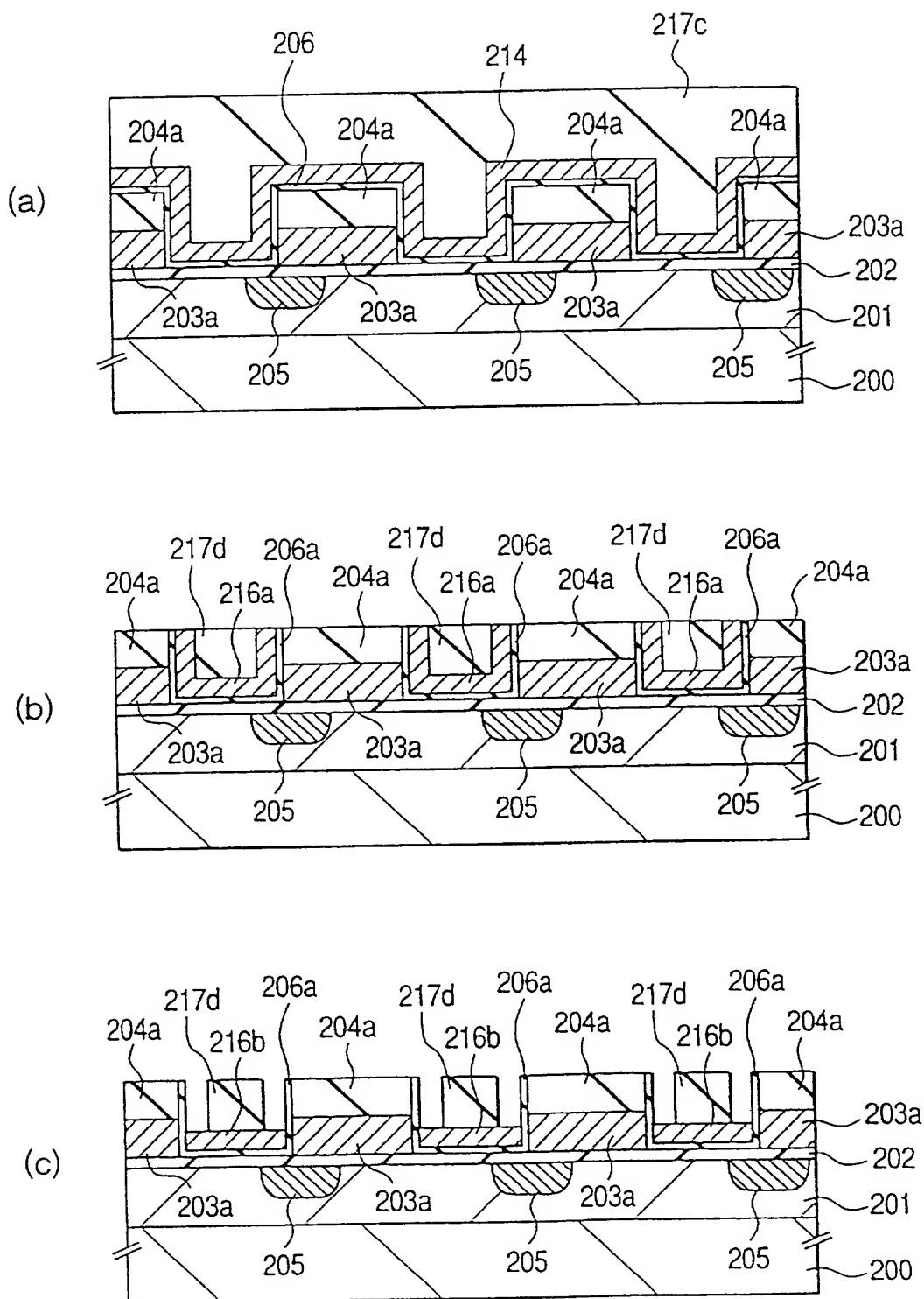


FIG. 15

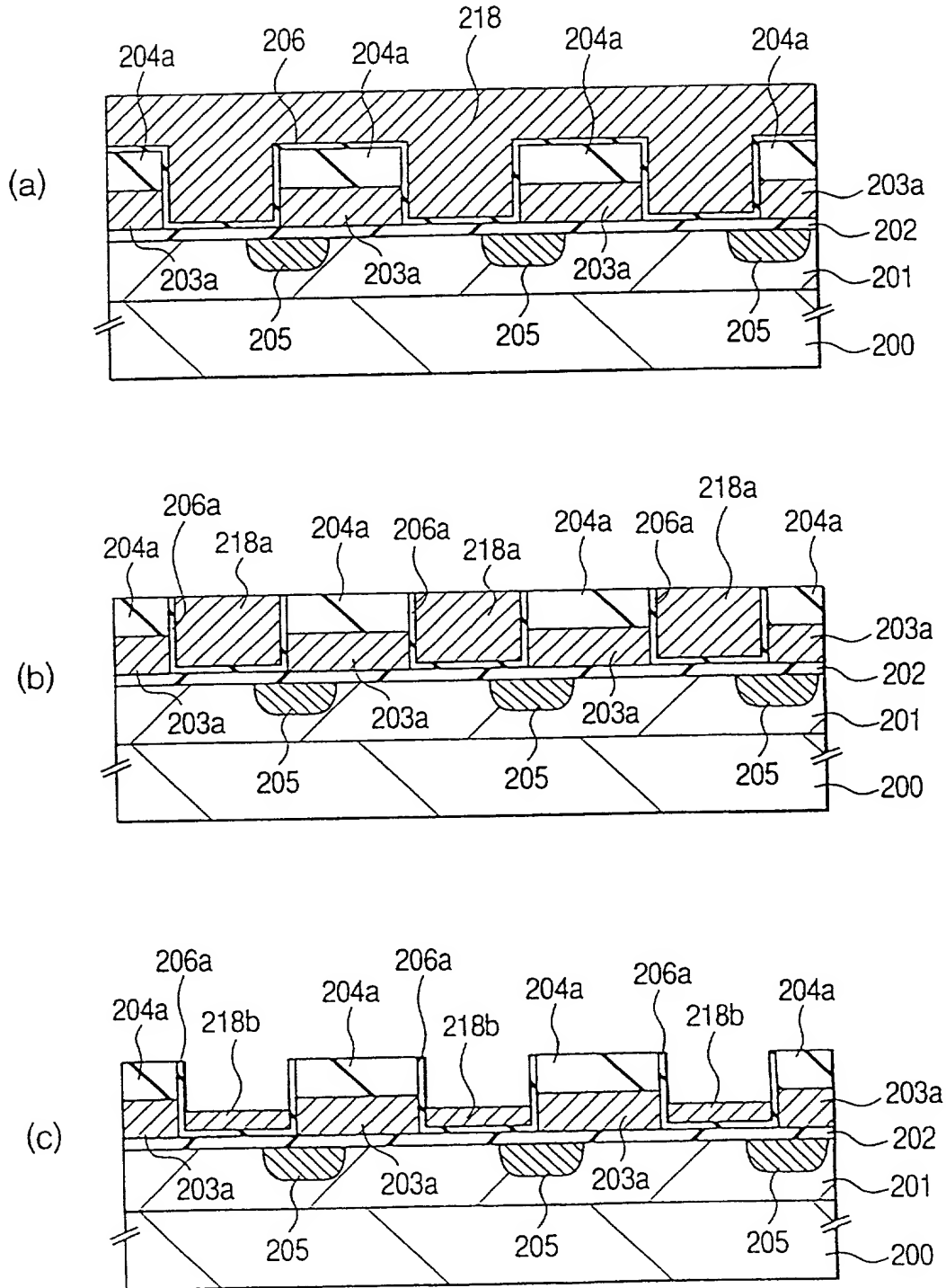


FIG. 16

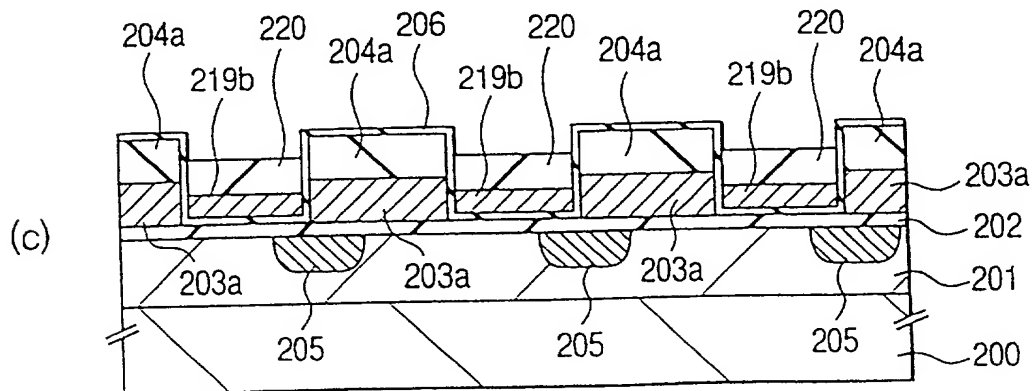
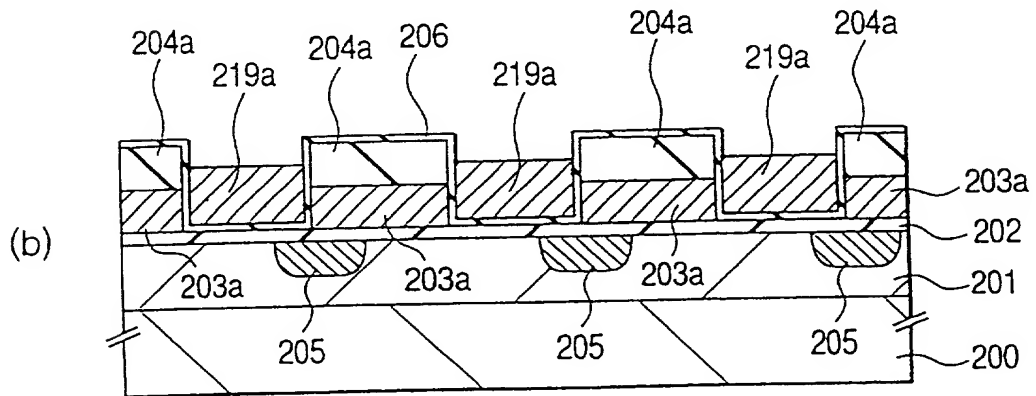
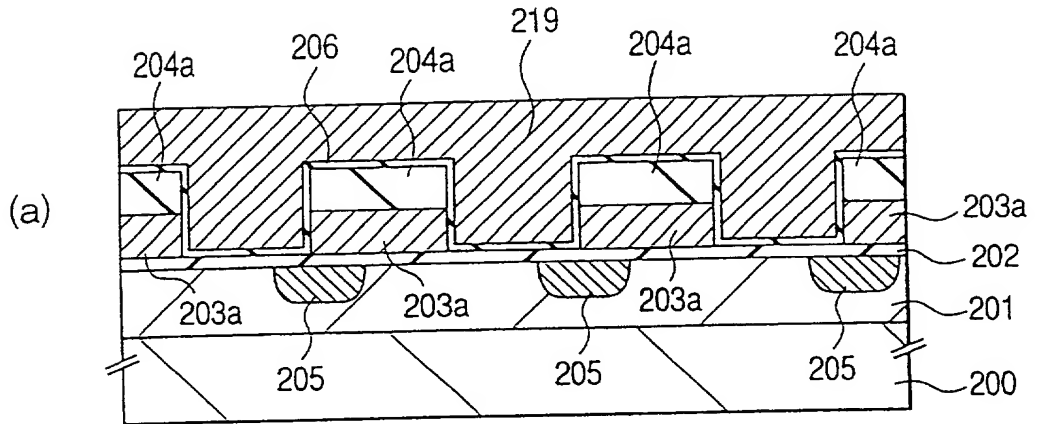


FIG. 17

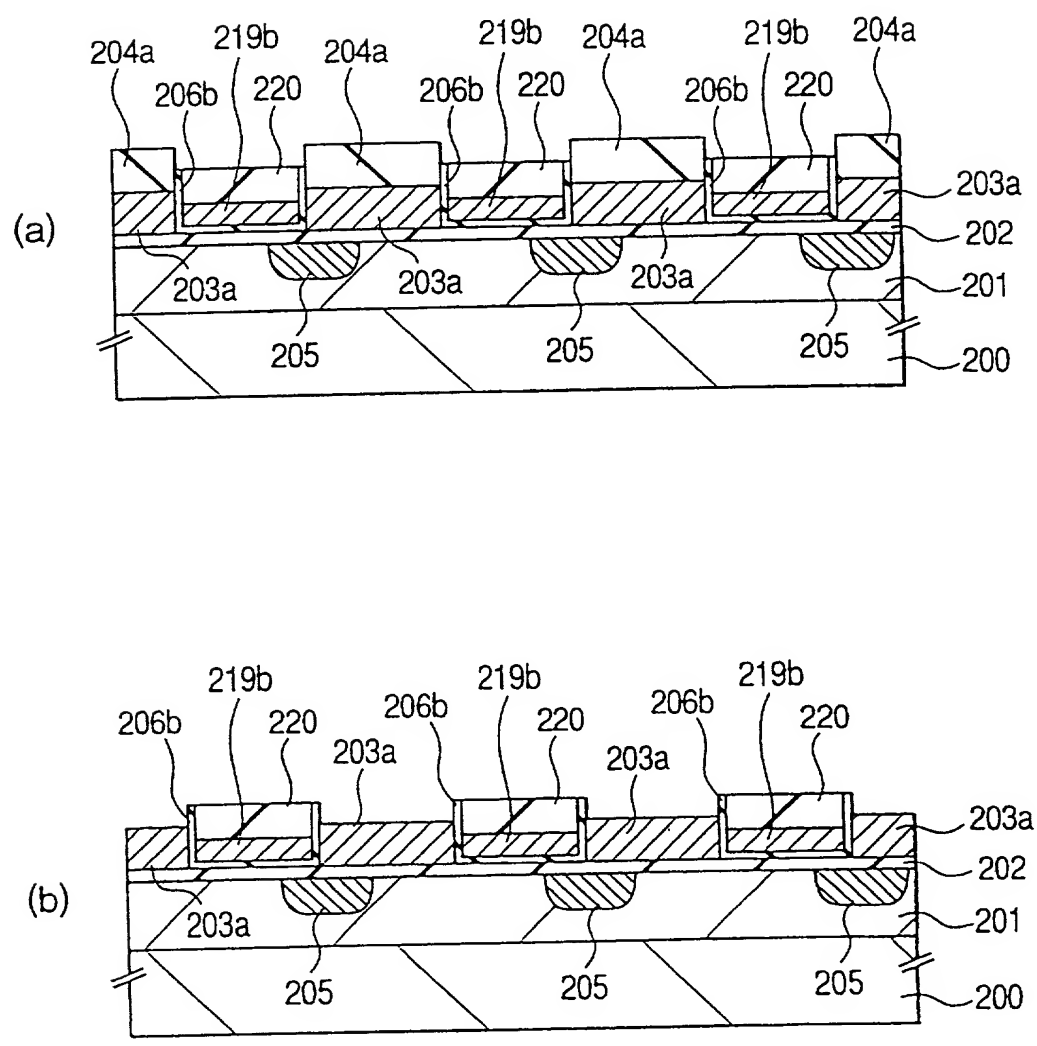


FIG. 18

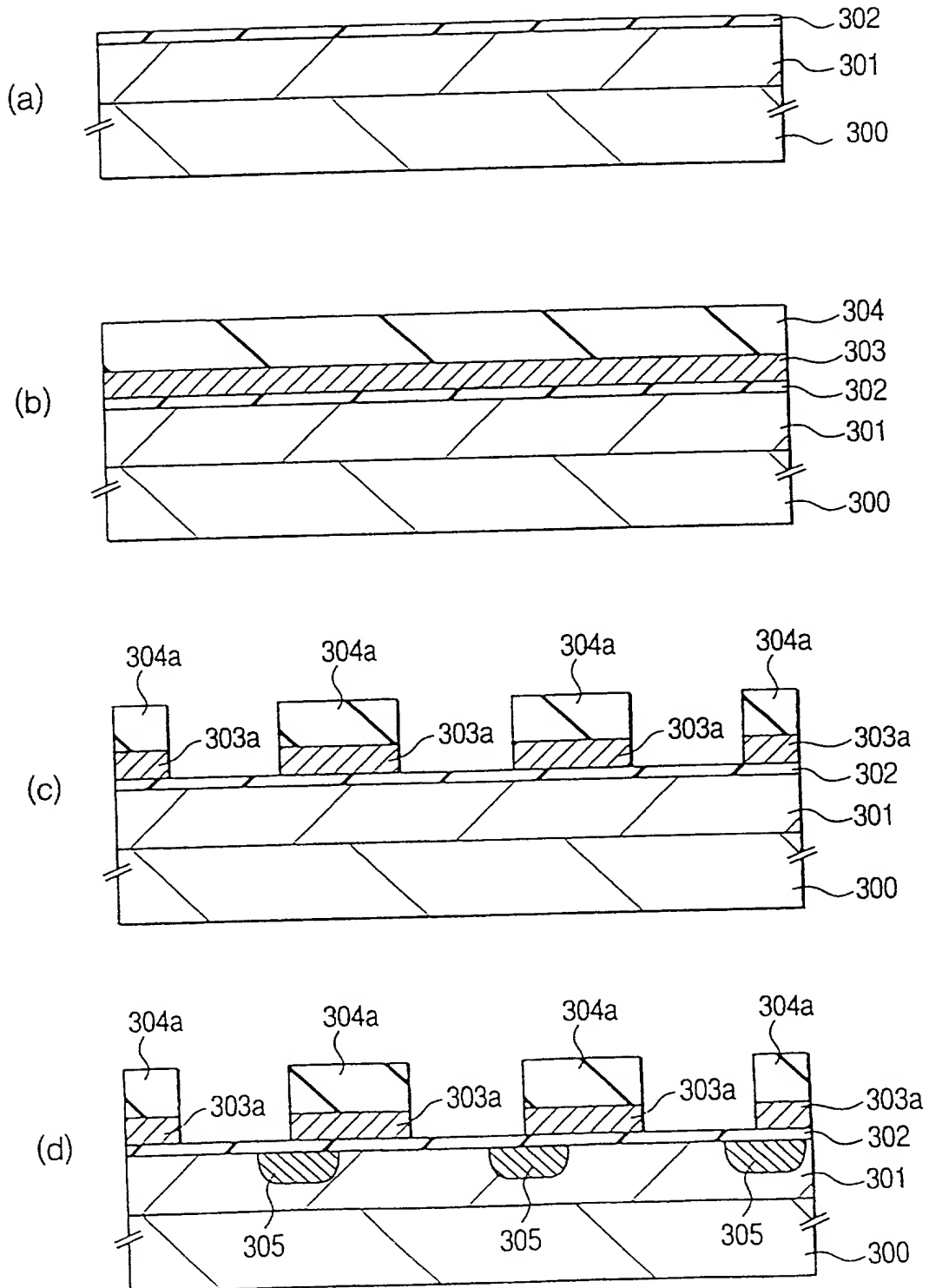


FIG. 19

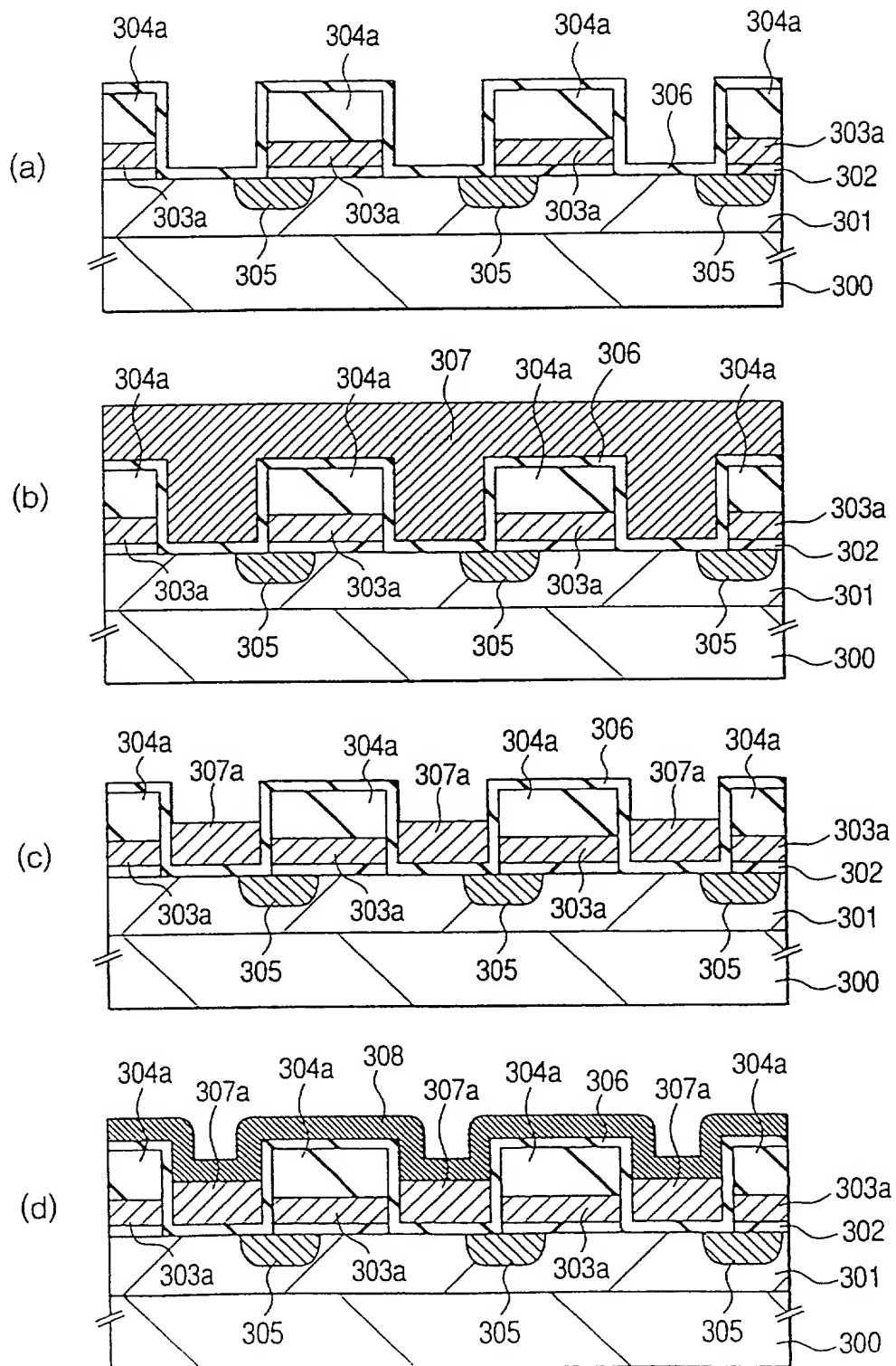


FIG. 20

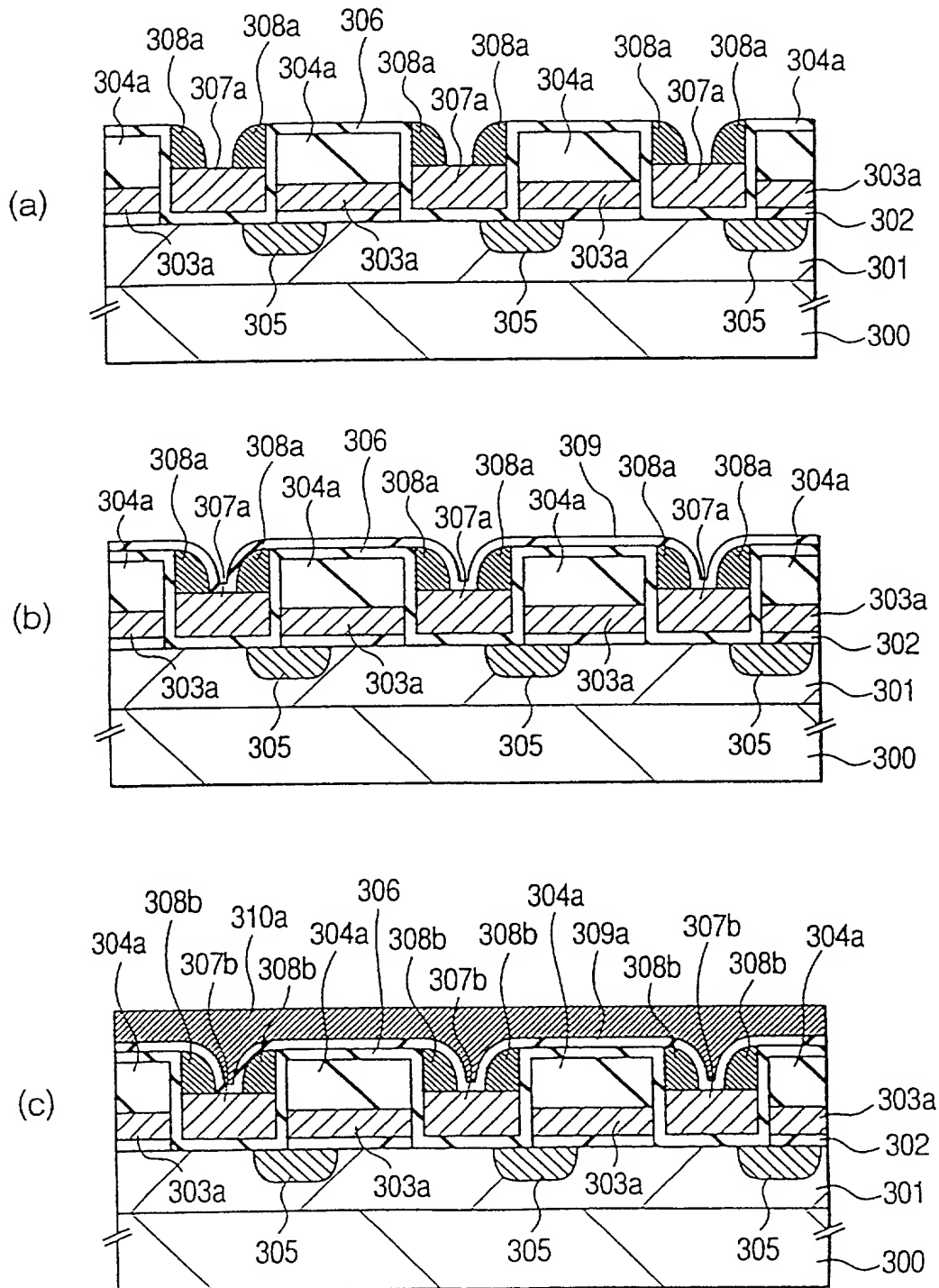


FIG. 21

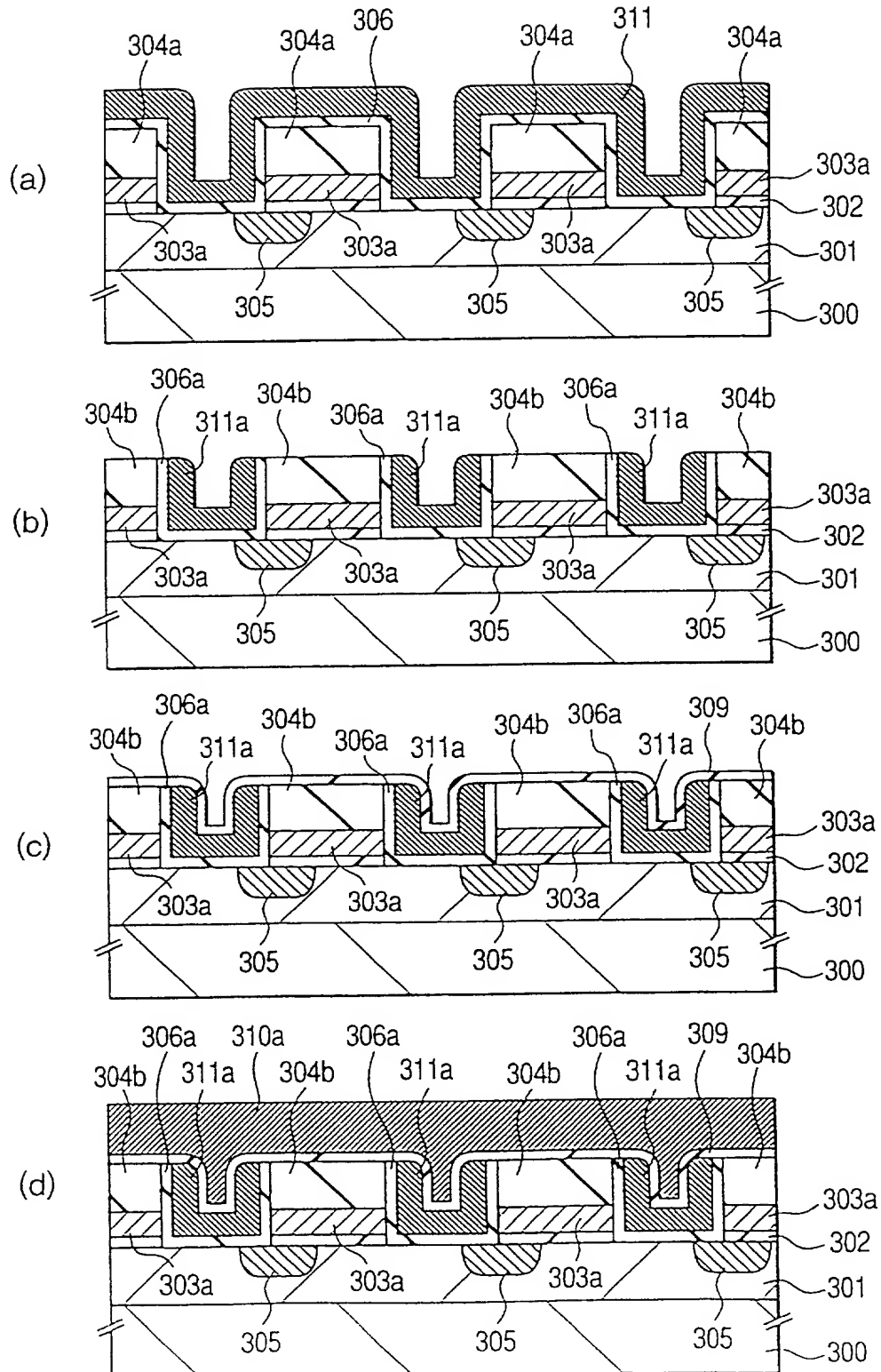


FIG. 22

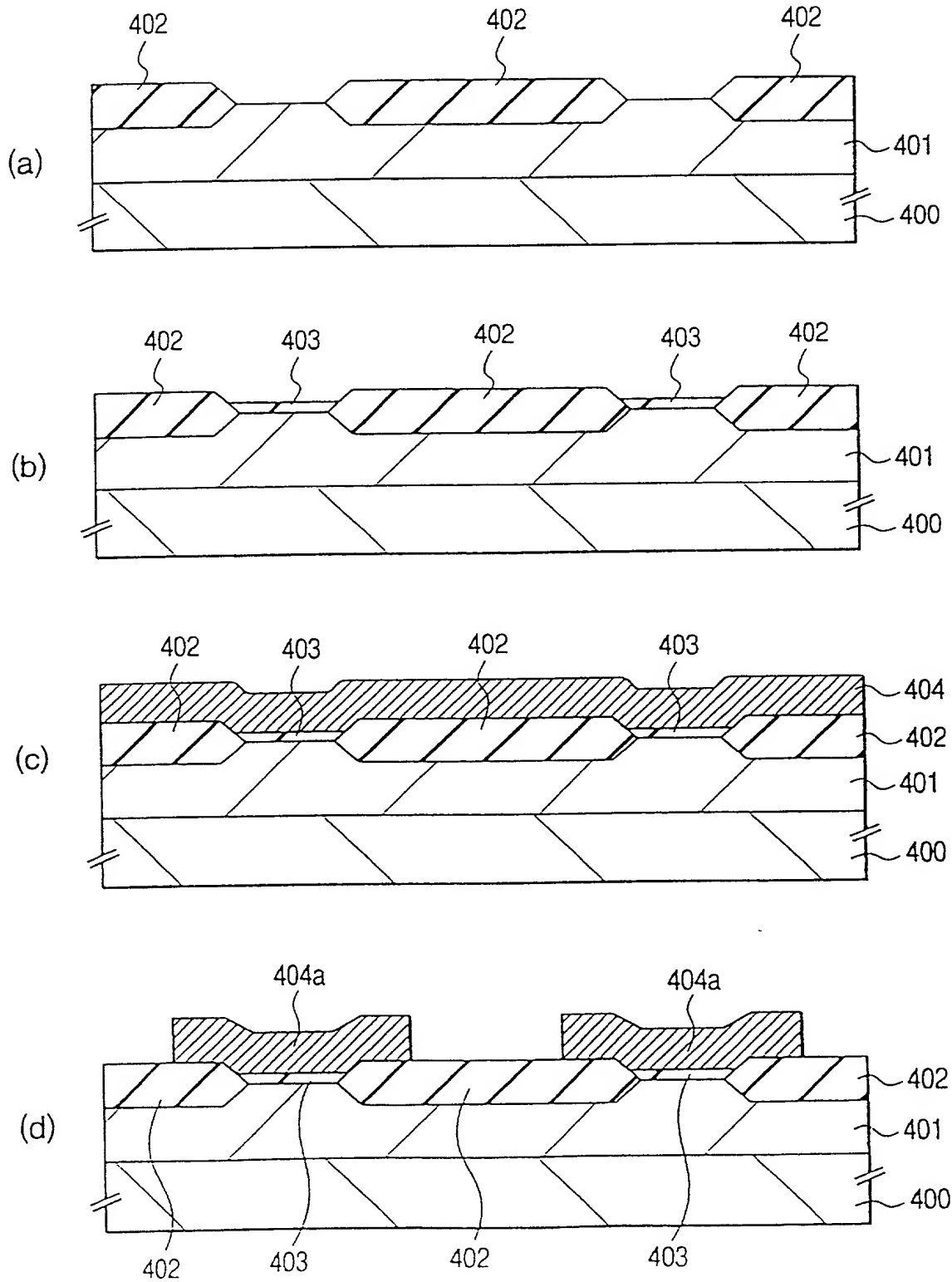


FIG. 23

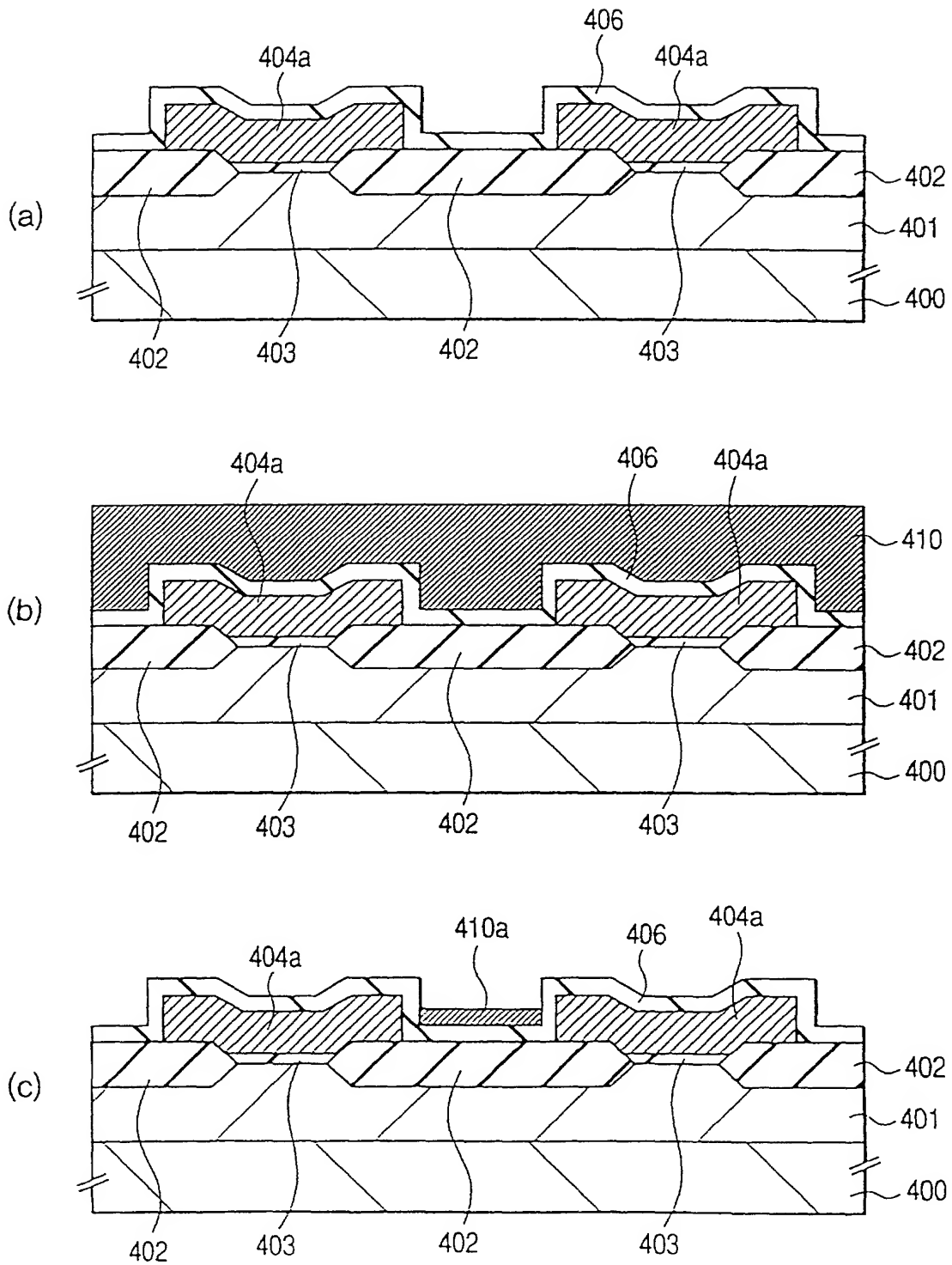
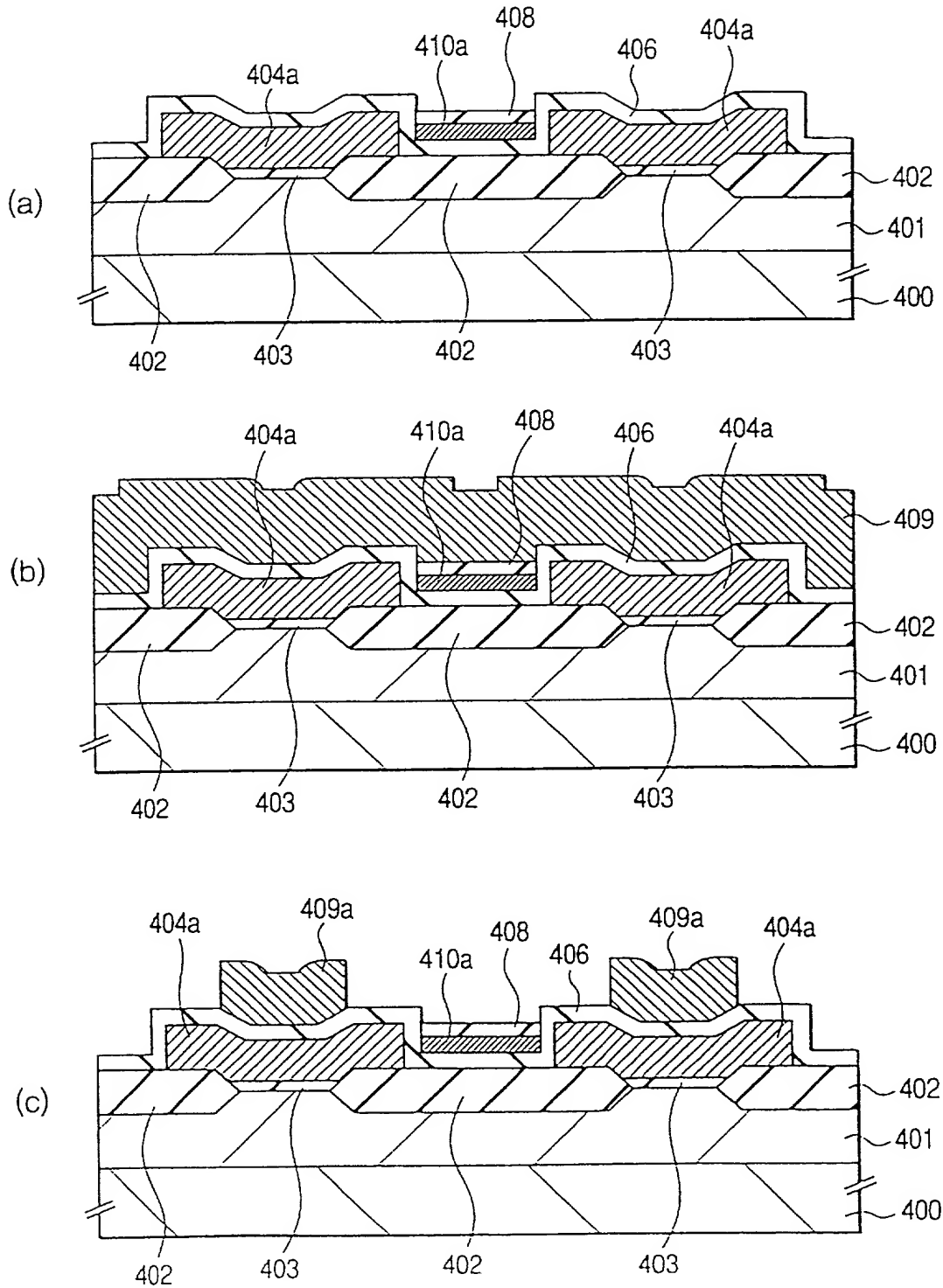


FIG. 24



Declaration and Power of Attorney For Patent Application

特許出願宣言書及び委任状

Japanese Language Declaration

日本語宣言書

下記の氏名の発明者として、私は以下の通り宣言します。

As a below named inventor, I hereby declare that:

私の住所、私書箱、国籍は下記の私の氏名の後に記載された通りです。

My residence, post office address and citizenship are as stated next to my name.

下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者であると（下記の名称が複数の場合）信じています。

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

AND PROCESS FOR PRODUCING THE SAME

上記発明の明細書（下記の欄で×印がついていない場合は、本書に添付）は、

The specification of which is attached hereto unless the following box is checked:

☐ 月 日に提出され、米国出願番号または特許協定条約国際出願番号を _____ とし、
(該当する場合) _____ に訂正されました。

☒ was filed on 8 / September / 2000
as United States Application Number or
PCT International Application Number
PCT/JP00/06146 and was amended on
8/Feb/2001 (if applicable).

私は、特許請求範囲を含む上記訂正後の明細書を検討し、内容を理解していることをここに表明します。

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

私は、連邦規則法典第37編第1条56項に定義されるとおり、特許資格の有無について重要な情報を開示する義務があることを認めます。

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

Japanese Language Declaration (日本語宣言書)

私は、米国法典第35編119条(a)-(d)項又は365条(b)項に基き下記の、米国外の国の少なくとも一カ国を指定している特許協力条約365(a)項に基き国際出願、又は外国での特許出願もしくは発明者証の出願についての外国優先権をここに主張するとともに、優先権を主張している、本出願の前に出願された特許または発明者証の外国出願を以下に、枠内をマークすることで、示しています。

Prior Foreign Application(s)

外国での先行出願

11-257990	Japan
(Number)	(Country)
(番号)	(国名)
(Number)	(Country)
(番号)	(国名)

私は、第35編米国法典119条(e)項に基いて下記の米国外特許出願規定に記載された権利をここに主張いたします。

(Application No.)	(Filing Date)
(出願番号)	(出願日)

私は、下記の米国法典第35編120条に基いて下記の米国外特許出願に記載された権利、又は米国外を指定している特許協力条約365条(c)に基き権利をここに主張します。また、本出願の各請求範囲の内容が米国法典第35編112条第1項又は特許協力条約で規定された方法で先行する米国外特許出願に開示されていない限り、その先行米国外出願書提出日より本出願書の日本国内または特許協力条約国際提出日よりの期間中に入手された、連邦規則法典第37編1条56項で定義された特許資格の有無に関する重要な情報について開示義務があることを認識しています。

(Application No.)	(Filing Date)
(出願番号)	(出願日)
(Application No.)	(Filing Date)
(出願番号)	(出願日)

私は、私自身の知識に基いて本宣言書中で私が行なう表明が真実であり、かつ私の入手した情報と私の信じていることに基き表明が全て真実であると信じていること、さらに故意になされた虚偽の表明及びそれと同等の行為は米国法典第18編第1001条に基き、罰金または拘禁、もしくはその両方により処罰されること、そしてそのような故意による虚偽の声明を行なえば、出願した、又は既に許可された特許の有効性が失われることを認識し、よってここに上記のごとく宣誓を致します。

I hereby claim foreign priority under Title 35, United States Code, Section 119(a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT international application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Priority Not Claimed

優先権主張なし

10 / September / 1999	<input type="checkbox"/>
(Day/Month/Year Filed)	
(出願年月日)	
(Day/Month/Year Filed)	<input type="checkbox"/>
(出願年月日)	

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below.

(Application No.)	(Filing Date)
(出願番号)	(出願日)

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s), or 365(c) of any PCT international application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of application.

(Status: Patented, Pending, Abandoned)	
(現況: 特許許可済、係属中、放棄済)	
(Status: Patented, Pending, Abandoned)	
(現況: 特許許可済、係属中、放棄済)	


I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Japanese Language Declaration (日本語宣言書)

委任状： 私は下記の発明者として、本出願に関する一切の手続きを米特許商標局に対して遂行する弁理士または代理人として、下記の者を指名いたします。(弁護士、または代理人の氏名及び登録番号を明記のこと)

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith (*list name and registration number*)

 Nelson H. Shapiro, Reg. No. 17,095, Mitchell W. Shapiro,
Reg. No. 31,568

書類送付先

Send Correspondence to:

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1751 Pinnacle Drive, Suite
McLean, Virginia 22102-3833

直接電話連絡先：(名前及び電話番号)

Direct Telephone Calls to: (*name and telephone number*)

Telephone: (703) 903-9000

Fax: (703) 610-8686

唯一または第一発明者名	Full name of sole or first inventor	<u>Takashi KOBAYASHI</u>
発明者の署名	Inventor's signature	<u>Takashi Kobayashi</u>
日付	Date	<u>11/6/2001</u>
住所	Residence	<u>Tokorozawa, Japan</u>
国籍	Citizenship	<u>Japan</u>
私書箱	Post Office Address	<u>c/o Hitachi, Ltd, Intellectual Property Group</u> <u>New Marunouchi Bldg. 5-1, Marunouchi 1-chome,</u> <u>Chiyoda-ku, Tokyo 100-8220, Japan</u>

(第二以降の共同発明者についても同様に記載し、署名をすること)

(Supply similar information and signature for second and subsequent joint inventors.)

第二共同発明者名	Full name of second joint inventor, if any	20
第二共同発明者の署名	Yasushi GOTO	
日付	Second inventor's signature	Date
	Yasushi GOTO	11/5/2001
住所	Residence	
	Kokubunji, Japan	JPX
国籍	Citizenship	
	Japan	
私書箱	Post Office Address	
	c/o Hitachi, Ltd., Intellectual Property Group New Marunouchi Bldg. 5-1, Marunouchi 1-chome, Chiyoda-ku, Tokyo 100-8220, Japan	
第三共同発明者名	Full name of third joint inventor, if any	30
第三共同発明者の署名	Tokuo KURE	
日付	Third inventor's signature	Date
	Tokuo Kure	11/7/2001
住所	Residence	
	Hinodemachi, Japan	JPX
国籍	Citizenship	
	Japan	
私書箱	Post Office Address	
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第四共同発明者名	Full name of fourth joint inventor, if any	40
第四共同発明者の署名	Hideaki KURATA	
日付	Fourth inventor's signature	Date
	Hideaki Kurata	11/5/2001
住所	Residence	
	Kokubunji, Japan	JPX
国籍	Citizenship	
	Japan	
私書箱	Post Office Address	
	c/o Hitachi, Ltd., Intellectual Property Group New Marunouchi Bldg. 5-1, Marunouchi 1-chome, Chiyoda-ku, Tokyo 100-8220, Japan	
第五共同発明者名	Full name of fifth joint inventor, if any	50
第五共同発明者の署名	Hitoshi KUME	
日付	Fifth inventor's signature	Date
	Hitoshi Kume	11/5/2001
住所	Residence	
	Musashino, Japan	JPX
国籍	Citizenship	
	Japan	
私書箱	Post Office Address	
	c/o Hitachi, Ltd., Intellectual Property Group New Marunouchi Bldg. 5-1, Marunouchi 1-chome, Chiyoda-ku, Tokyo 100-8220, Japan	

(第六以降の共同発明者についても同様に記載し、署名をすること)

(Supply similar information and signature for sixth and sequent subsequent joint inventors))

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第六共同発明者名	Full name of sixth joint inventor, if any	
	Katsutaka KIMURA 50	
第六共同発明者の署名	日付	Sixth inventor's signature Date
		<i>Katsutaka Kimura</i> 11/5/2001
住所	Residence	
	Akishima, Japan JPX	
国籍	Citizenship	
	Japan	
私書箱	Post Office Address	
	c/o Hitachi, Ltd., Intellectual Property Group New Marunouchi Bldg. 5-1, Marunouchi 1-chome, Chiyoda-ku, Tokyo 100-8220, Japan	
第七共同発明者名	Full name of seventh joint inventor, if any	
	Syunichi SAEKI 70	
第七共同発明者の署名	日付	Seventh inventor's signature Date
		<i>Syunichi SaeKi</i> 11/5/2001
住所	Residence	
	OME, Japan JPX	
国籍	Citizenship	
	Japan	
私書箱	Post Office Address	
	c/o Hitachi Device Engineering Co., Ltd., 3681, Hayano, Mobara-shi, Chiba 297-8581, Japan	
第八共同発明者名	Full name of eighth joint inventor, if any	
第八共同発明者の署名	日付	Eighth inventor's signature Date
住所	Residence	
国籍	Citizenship	
私書箱	Post Office Address	
第九共同発明者名	Full name of ninth joint inventor, if any	
第九共同発明者の署名	日付	Ninth inventor's signature Date
住所	Residence	
国籍	Citizenship	
私書箱	Post Office Address	

(第十以降の共同発明者についても同様に記載し、署名をすること)

(Supply similar information and signature for tenth and subsequent joint inventors.)